DØ Upgrade Electronics
L2STT Trigger
System Architecture Proposal v1.0

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August 31, 1999

Abstract

This document describes a proposed implementation of the L2STT trigger for the
DØ upgrade. A 9U x 400mm generic motherboard with all required I/O is used as the
base for all custom modules. Custom mezzanine boards are used to implement specific
functions. VIPA subracks (crates) with customized P3 backplanes house all modules.

This document builds on our previous description of a generic motherboard by
proposing specific choices for all data links in the system. LVDS serial links are used
for most system interconnections, and industry-standard PCI busses are used for most
board-board connections. All design decisions reflected in this document are still sub-
ject to change.

1 System Overview

The L2STT (Level 2 Silicon Tracking Trigger) is a preprocessor subsystem for the Level 2
DØ trigger, which matches "roads" from the CFT (Central Fiber Tracker) with hits from
the SMT (Silicon Microstrip Tracker). Centroids are calculated from SMT hits, and tracks
fit to the clusters. The resulting information is provided to L2 and L3.

The system as proposed here is implemented as six crates, each servicing two SMT sectors.
An overview showing the modules and interconnections within a crate is shown in Figure 1.

1.1 Data Flow

CFT data is processed into roads by the L1CTT (Level 1 Central Tracking Trigger), and
transmitted to the FRC (Fiber Road Card) on an optical fiber link (using HP G-Link
protocol). The data is received via a rear-mounted VTM (VRB Transition Module). A DØ
standard SCL (Serial Command Link) receiver mezzanine card provides clock, trigger and
timing information which is used by all modules in the crate. The FRC buffers the road
Figure 1: **DØ L2STT Crate.** (15) 9Ux400mm modules comprise the system, with space for additional modules for monitoring and control. Shaded (gray) modules are based on a generic motherboard with custom daughterboards. P0/P1/P2 backplane is standard VME64x[1] (or VME64xP/VIPA)[2]. P3 Backplane is a variation of the DØ SVX-II J3 backplane. Note that VTM transition modules are not shown.

information and combines it with relevant SCL events and transmits this over point-to-point links to the entire crate.

Each **STC** (Silicon Trigger Card) receives SMT data via a VTM. Each VTM has 4 fiber receivers, each servicing two SMT detector readout channels. One crate contains 9 STC’s, servicing two sectors. The STC also receives the L1CTT road information. The STC combines SMT hits into clusters, matches the clusters to roads, and transmits the resulting data over a point-to-point link to a **TFC** (Track Fit Card) for fitting. Z cluster information from the stereo strips is transmitted to a **ZVC** (Z-Vertex Card), also over a point-to-point link. The STC also buffers all data on-board for VME readout to Level 3.

A TFC receives $\rho$ cluster information from a number of STCs, and also receives the L1CTT roads from the FRC. Fitted track data is transmitted by Cypress Hot-Link to the L2CTT (Level 2 Central Tracking Trigger). Track information is also buffered on-board for VME readout to Level 3. Each TFC is currently envisioned to handle one sector, receiving
\( r^\phi \) cluster information from 5 STCs. This could be changed easily if more TFCs are required.

A ZVC receives \( Z \) cluster information from a number of STCs and transmits it to a global \( Z \) vertex system (possibly with local processing). Details of this part of the system are not well defined.

Level 3 data is read out over the VME bus by a D\( \emptyset \) standard VBD (VME Buffer Driver) module.

### 1.2 Crate/Backplane Requirements

We propose to use VTM\$s in the crate, which implies a few things:

- VME64x 9Ux400mm\[3\] crate, with provisions for 9Ux120mm transition modules
- SVX J3 backplane for all slots where VTM\$s will be used

Since “VIPA standard” crates are widely used in the experiment, we propose to adopt this standard also.

### 1.3 Point-to-Point Links

The system uses many identical point-to-point links for interconnection. All support at least 26.5MHz transfer of 32-bit words. Three link transmitters or receiver plus control logic will be implemented on a single PC-MIP mezzanine board.

### 2 9U Motherboard

#### 2.1 Introduction

As was recently pointed out by our collaborators, there are a significant number of custom modules in the L2STT design. They share common requirements for internal and external interfaces. We summarize those requirements here and propose a common motherboard.

The required I/O for the motherboard is summarized in Table 1. Most I/O can be accommodated using either PC-MIP mezzanine cards or D\( \emptyset \) Standards. A mechanical sketch of the proposed motherboard is shown in Figure 2.

#### 2.2 Motherboard Logic

A block diagram of the motherboard is shown in Figure 3. The subsections are described in more detail below.

**Point-to-Point Link I/O**

Six identical mezzanine boards hold the point-to-point link receiver or transmitter boards. These mezzanine boards will be fully-compliant with the PC-MIP standard and can therefore be installed on off-the-shelf carrier boards for debugging and tester applications.
<table>
<thead>
<tr>
<th>SCL Input</th>
<th>DØ standard SCL mezzanine card. PC-MIP mechanics, non-compatible pinout.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fiber G-link</td>
<td>DØ standard VTM transition module provides 4 inputs.</td>
</tr>
<tr>
<td>Point-to-Point Links</td>
<td>26.5MHz x 32-bit transmitters and receivers will be implemented on 3-channel PC-MIP modules. The physical links will most likely be 21-bit LVDS Channel Links operating at 53MHz.</td>
</tr>
<tr>
<td>VME Interface</td>
<td>A standard 32-bit VME slave interface is required. This may be implemented with either an off-the-shelf interface IC or an FPGA.</td>
</tr>
<tr>
<td>Buffer Control</td>
<td>Dedicated I/O to SVX J3 backplane “local bus”.</td>
</tr>
<tr>
<td>Trigger init/status</td>
<td>Dedicated user lines on J0 or J2</td>
</tr>
</tbody>
</table>

Table 1: L2STT Motherboard I/O.

Point-to-point link transmitters or receivers are grouped on two 32-bit wide PCI busses. A PCI-to-PCI bridge provides an optional interconnection between the busses. The primary bus master for each bus resides on one of the logic mezzanine boards.

The link receiver logic is designed such that a single PCI-bus block read may be used to harvest data from an “event” with various-sized blocks from each link. Thus no specific multiplexing is required. A detailed description of this logic is contained in Section 2.3.1.

SCL Receiver

The SCL receiver is implemented as a DØ standard on a PC-MIP-like mezzanine board. Unfortunately this board is not at all compatible with the PC-MIP standard pinout. Thus, a separate set of connectors is provided, offset from the first PC-MIP link receiver site. The relevant SCL signals are carried via dedicated connections to top logic daughterboard position.

VTM Inputs

A dedicated connection carries two G-Link fiber input channels to each of the logic mezzanine boards. Some simple processing (latching, error checking) of the data may be performed on the motherboard.

The motherboard will also provide control and monitoring of optical link status via the micro-controllers on the VTMs.

Level 3 Buffering

Data is produced in many parts of the STT system which must be stored and transmitted to Level 3/DAQ. This data is stored in FIFOs on the logic mezzanine boards where it is
produced, and then read out via PCI bus 3 to a dual-port memory buffer on the motherboard. The central buffer controller on the FRC transmits messages to the other modules via the local bus on the SVX J3 backplane.

The Buffer Control logic block (see Figure 3 is master of PCI bus 3, which is used to read Level 3/DAQ data from the logic mezzanine boards. The data is stored in a dual-port memory, at a location designated by the central buffer controller. Messages are received via a dedicated connection to the SVX J3 backplane. Note that on the FRC, the central buffer controller is located on a logic mezzanine board. In addition, the FRC receives its own messages and stores Level 3/DAQ data.

**VME Interface**

The VME bus is used for initialization and monitoring, plus readout of data to Level 3/DAQ. Level 3 data is read from the dual-port memory directly. Initialization and monitoring is performed via a VME-to-PCI bus bridge, which allows direct access to logic mezzanine board functions from the VME environment.

**JTAG**

JTAG is implemented extensively for testing and FPGA programming. A JTAG scan path covers all programmable devices on the motherboard and mezzanine boards, allowing complete testing (even *in situ*) of all electrical interconnections. In addition, most logic devices may be reprogrammed via JTAG.

JTAG access is provided by a dedicated connector, and also via a simple JTAG controller accessed via VME, for *in situ* access.

### 2.3 Mezzanine Boards

As shown in Figure 2, the proposed motherboard accommodates 6 PC-MIP[4] mezzanine boards for I/O along the front panel, and four PMC[5] mezzanine boards for logic.

#### 2.3.1 Point-to-Point Link Receivers

Figure 4 shows a 3-channel link receiver. In most applications, data must be harvested as variable-size blocks from various link receivers to form an event. To perform this operation efficiently, the bus master must be able to perform a single block read of the entire event. This is implemented using a token-passing scheme similar to the “Chained Block Transfer” described in the VIPA standard[2]. All receiver cards respond to the same PCI address for data readout, and each provides it’s data for the next event number, then passes a token to the next daughterboard via a dedicated connection. This effectively moves the event building function to the link receiver board.

The receiver boards can also operate in a simpler mode where each link’s data may be read separately. Parity error checking is performed on the link receiver, and an error bit is set in the data to indicate presence of link errors.
The receiver boards are designed to be compliant with the PC-MIP and PCI local bus standards, so they may be installed on a commercial, off-the-shelf processor board for testing and debugging.

2.3.2 Point-to-Point Link Transmitters

The point-to-point link transmitter is much simpler than the receiver. It contains a data FIFO for each link. The 3 transmitters on a board can be configured to operate in parallel, “broadcast” mode or independently. Parity is computed and added to each transmitted word.

The transmitter boards are designed to be compliant with the PC-MIP and PCI local bus standards, so they may be installed on a commercial, off-the-shelf processor board for testing and debugging.

2.3.3 Logic Boards

Each motherboard holds two logic mezzanine boards, which are double-sized, extended CMS boards, as shown in Figure 5. Each board may have one or two PCI bus interfaces. Two connectors are required for each 32-bit PCI bus; a third is reserved for possible expansion to 64 bits. Other connectors are user-defined under the PMC standard and are used for the dedicated interconnections for Level 3 buffer control, SCL and VTM data.

Mechanically, the boards are foreseen to be 150x150mm for prototypes and 150x250mm for the final design. The 150mm long boards can be installed in off-the-shelf commercial PMC carrier boards, while the longer boards are accommodated on our custom motherboard. It may be advantageous to move the user-defined connectors to another location to allow their use for prototyping.

3 Summary

We have described here a proposed system architecture for the L2STT. It makes extensive use of existing standards and modules (VIPA crates; PCI busses; PC-MIP, PMC and SCL mezzanine boards; VTM and VRB modules). Point-to-point links are used for most system interconnections. A common motherboard is used for all custom L2STT modules.

The extensive use of the PCI bus should permit the design, fabrication, and testing of modules to proceed independently. Commercial processors or carrier boards are available which accommodate PC-MIP and PMC modules.

Thus, we advocate that this solution or a similar one be adopted for the L2STT design.
References


[5] *PCI Mezzanine Cards IEEE P1386.1/2.0 4/4/95*

Figure 2: **Generic Motherboard for L2STT.** Approximately to scale. Mezzanine boards on front-panel are PC-MIP standard, while logic mezzanine boards are CMC “double extended” standard. Logic boards could clearly be enlarged at our discretion if needed.
Figure 3: **Motherboard Block Diagram.** Most interconnections are PCI local bus standard. Three separate busses are implemented to avoid bottlenecks. “M” indicates a PCI master/target interface while “T” indicates a PCI target-only interface. Unlabeled connections are dedicated interconnections carried on user-defined pins.
Figure 4: **Point-to-Point Link Receiver.** A PC-MIP card holds 3 link receivers and readout logic.
Figure 5: **Logic Mezzanine Board** is a double-extended PMC type board. Connectors labelled “PCI” are for industry-standard PCI busses. Other connectors are for dedicated functions (user-defined)