Event-Building Functions

Link Receiver Board(s)

Logic Board

Event Fragments combined during PCI bus transfer

Block Diagram

LVDS Serial Recievers
(i.e. National Semi "Channel Link")

PCI Bus
(32 bit)

DS90CR286 Link A  →  FIFO 32K x 36

DS90CR286 Link B  →  FIFO 32K x 36

DS90CR286 Link C  →  FIFO 32K x 36

128k byte buffers
(enough for 16 D0 events)

ALTERA
(EPS9320 i.e.)

FPGA
(PCI Interface and readout/monitor logic)

Flags

Control