Generic Hardware

Presentation Outline

Generic Hardware Motivation

9U VME Motherboard
  Features and Layout Sketch
  Block Diagram
  Status and Schedule

PC-MIP Link Receiver Board
  Features and Block Diagram
  Implementation, Status, Schedule

PC-MIP Link Transmitter Board
  Features, Diagram, Status

Data Flow on Each STT Module
Review of L2STT

**Why Use "Generic" Hardware?**

L2STT modules have many common requirements:

- VME Interface, 9U form factor
- Fast I/O (16 bits * 53MHz = 850 Mbits/sec)
- Buffered readout to Level 3 / DAQ
- CPU access for downloading and monitoring

L2STT modules will use 3 "generic" components:

- 9U x 400mm VME motherboard
- 3-channel LVDS link transmitter board
- 3-channel LVDS link receiver board

Each module will have one large mezzanine board with custom processing and monitoring logic.

Other advantages of generic hardware:

- Reduced overall engineering cost
- Debug using "known good" platform
- Easier maintenance, smaller spares inventory
Review of L2STT

Generic 9U VME Motherboard

9Ux400mm VME64xP (VIPA) Module

SCL Receiver Mezzanine

Logic Board (2X "Double-Extended" CMC format)

Point-to-Point LVDS Transmitters or Receivers (PC-MIP standard)
Review of L2STT

Generic 9U VME Motherboard

Current Status

All I/Os pinouts specified
Most logic functionality is defined by standards (VME, PCI, JTAG) (except L3 buffer control...)
All Connector Placement Defined

Schedule

Detailed Engineering Design to begin 4/1
Prototypes Available by 8/1/00
Review of L2STT

PC-MIP Link Receiver Board

Event-Building Functions

Link Receiver Board(s)

Logic Board

Event Fragments

LVDS Serial Receivers
(i.e. National Semi "Channel Link")

128k byte buffers
( Enough for 16 D0 events)
**Implementation Details**

PC-MIP (PCI bus Module Industry-Pack) standard chosen provides 32 bit PCI bus interface in convenient format

Receiver buffer in 36-bit FIFO (sizes 1k-128k available)
All logic in a single Altera MAX9000 fast FPGA
Extensive error correction/recovery/monitoring built in

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**Current Status and Plans**

Engineering design now underway - complete by 3/3/00 (PCB design, FPGA program)

Prototypes expected by 3/24/00
Major Features

Single FIFO feeding 3 LVDS transmitters in parallel
Automatic formatting of blocks (Header, Data, Trailer)
FIFO repeat (free-run and triggered) for system test
PC-MIP standard module with 32-bit PCI interface

First Prototypes expected ~ 5/1/00

Block Diagram
Review of L2STT

Generic 9U VME Motherboard

Data Flows in STT Modules