HCAL/HF Readout

DCC Module Buffering

From 18 HTRs (Link Receivers)

**BUFFER SIZES**

- 100 events
  - ~ 10k bytes

- 1000 (average) events
  - ~ 2Mbytes

**Diagram:**

- TTC
- PCI Busses on DCC
- Processing FPGA
- Dual Port Memory
- Protocol FPGA
- Fiber Transmitter
  - Fiber to RUI
    - (surface counting house)