**HCAL Trigger/DAQ**

**Introduction**

System Design Fixed as shown

HTR Cards (Maryland)
read out 32 HCAL channels each

DCC (Boston)
bUILds events for DAQ (DDU)

HRC (Illinois) includes CPU
TTC fanout, fast+slow monitoring

This presentation:

Brief System Overview
HTR review
some DCC details and status
USCAMS HCALTriDAS

HCAL TRIGGER and READOUT Card

- All I/O on front panel
  - Level 1 Trigger Tower data outputs:
    - 8 shielded twisted pair
    - 4 per single 9-pin D connector
  - TTC input:
    - From TTCrx on HDC, ala ECAL
  - Raw data Inputs:
    - 16 digital serial fibers from QIE
    - 1 serial twisted pair with TTC information
  - DAQ data output to DCC:
    - Single connector running LVDS

- FPGA logic implements:
  - Level 1 Path:
    - Trigger primitive preparation
    - Transmission to Level 1
  - Level 2/DAQ Path:
    - Buffering for Level 1 Decision
    - No filtering or crossing determination necessary
    - Transmission to DCC for Level 2/DAQ readout
HCAL Trigger/DAQ

Data Concentrator (DCC) Block Diagram

Point-to-point Links from HTR Cards

Event Builder

Output FIFOS

Fast Monitoring

Spy Memory

"1000 Event" DDU buffer

Trigger Data Buffer

Front-End Link Transmitter (PMC)

VME-PCI Universe II

TTC Signals from HRC

Monitoring Signals to HRC

to Trigger Data Conc.

PC1 Bus 1

PC1 Bus 2

PC1 Bus 3
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Single Channel of DCC Logic

PCI Bus 1
PCI Bus 2
PCI Bus 3

PCI Master
FIFO
Event Builder
Trigger FIFO
Monitor FIFO
Spy FIFO
DAQ Buffer "1000 Event" Memory
PCI Master/Target

Trigger Link Tx
Monitor Link Tx
Local Bus
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CMS Week 2000 May
Single Channel of DCC Logic

Master PCI FIFO
Master PCI FIFO
Generic Motherboard Physical Layout (for DCC)
- 33MHz x 32 bit transfer rate on link and PCI interface
- on-the-fly ECC (correct single-bit errors, detect multi-bit)
- on-board event-building, event# checking

**Block Diagram**

**Link Receiver Board(s)**

**Logic Board**

Event Fragments combined during PCI bus transfer

**LVDS Serial Receivers**
(i.e. National Semi "Channel Link")

- DS90CR286 Link A
- DS90CR286 Link B
- DS90CR286 Link C

128k byte buffers

**PCI Bus**
(32 bit)

FPGA
(PCI Interface and readout/monitor logic)

**ALTERA**
(EPS9320 i.e.)

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HCAL Trigger/DAQ

Link Receiver Board (PC-MIP)

PC-MIP format 3-channel Link Receiver

90 mm

47 mm

32 bit 33MHz PCI

Current Status (5 May) - prototypes under test.
Basic functions work as expected.
Matching transmitter PCBs due back this week.
HCAL DCC demonstrator will be ready by end of 2000

Features:

- Generic 9U VME motherboard with PCI busses
- High-speed point-to-point link receivers with event building
- Prototype DCC logic on mezzanine board (multi-PMC)
- PMC site with 33MHz x 32 or 64-bit PCI for DAQ interface

These features may be changed in later versions, but we are committed to the PCI bus!