- 33MHz x 32 bit transfer rate on link and PCI interface
- on-the-fly ECC (correct single-bit errors, detect multi-bit)
- on-board event-building, event# checking

```
Block Diagram

LVDS Serial Receivers
(i.e. National Semi "Channel Link")

<table>
<thead>
<tr>
<th>DS90CR286</th>
<th>FIFO 32K x 36</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link A</td>
<td></td>
</tr>
<tr>
<td>Link B</td>
<td></td>
</tr>
<tr>
<td>Link C</td>
<td></td>
</tr>
</tbody>
</table>

128k byte buffers

PCI Bus
(32 bit)

ALTERA
(EPS9320 i.e.)

FPGA
(PCI Interface and readout/monitor logic)

Logic Board

Event Fragments combined during PCI bus transfer

Event Fragments

Link Receiver Board(s)