Simplifications for Rapid Prototyping:

Initially just 3 HTR inputs (can expand to 9)
No monitoring or "trigger DAQ" dedicated outputs
Simple S-Link output for DAQ (may omit on first prototype)
No automatic error recovery logic (requires CPU intervention)
TTCRx daughterboard on DCC (no TTC fanout)
Re-use existing designs where possible
FIFOs will be external to FPGAs

Planned Implementation:

3 FPGAs with Altera PCI cores + other logic
  PCI-MT/32 core used for other projects and understood
  Altera ACEX low-cost FPGA family is a good fit

Single large processing FPGA for fanout to various streams

  Input logic reads events from FIFO and performs error checking
  Output logic (data-driven, identical for each stream)
    selects events based on prescaling
    or header bits and writes to FIFO or FIFO-like interface