HCAL FE/DAQ Overview

DDU/FED
LEVEL 1 TRIGGER

16 800Mbit/s fiber per HTR

18 HTRs per HCAL Readout Crate

TTC

L1 Accept

DAQ Crate
(in UXA)

Trig Primitives calculated, sent to L1 Calo Trig

Level 2 data sent to RUI

Level 1 TRIGGER

Readout Box (RBX)
(On detector)

QIE (ADC) sends 1 charge sample Per BX to UXA via GOL optical link

CONTROL MODULE

FE READOUT MODULE

HPD

Shield Wall

VR

TX

800 Mbit/s

1 Gbit/s
These parameters drive the design and project cost:

- **HCAL Channels and topology determines**
  - Total channel count
  - Total number of trigger towers (includes calibration fibers)
    - Need to understand 53° Overlap region, high rad region, fiber cabling, etc.
  - QIE Readout parameters determine
    - Number of channels/card:
      - 3 channels/fiber seems likely
    - Total number of cards to build
  - Data rates
    - Assume 100kHz Level 1 accepts
    - Occupancy estimated to be 15% at L=10^{34}
    - Determines buffer sizes
  - Level 1 trigger crossing determination
    - Under study (Eno, Kunori, et al.)
    - Determines FPGA complexity and size (gates and I/O)

<table>
<thead>
<tr>
<th>Region</th>
<th>Towers</th>
<th>Fibers</th>
<th>Trigger Towers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barrel</td>
<td>4,968</td>
<td>2,304</td>
<td>2,304</td>
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<tr>
<td>Outer</td>
<td>2,280</td>
<td>1,140</td>
<td>0</td>
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<tr>
<td>Endcap</td>
<td>3,672</td>
<td>1,836</td>
<td>1,728</td>
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<tr>
<td>Forward</td>
<td>2,448</td>
<td>1,206</td>
<td>216</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>13,368</strong></td>
<td><strong>6,486</strong></td>
<td><strong>4,248</strong></td>
</tr>
</tbody>
</table>
HCAL Readout Crate

- **Receiver and pipeline cards:**
  - 18 HCAL Trigger / Readout (HTR) Cards per crate
    - Raw FE data input from RBX
    - Level 1 Trigger Primitives output
    - Level 2 Data output to DCC each L1A

- **Data Concentrator:**
  - 1 DCC card (Data Concentrator Card)
    - Receives and buffers L1 accepts for output to L2/DAQ

- **Crate controller:**
  - 1 HRC card (HCAL Readout Control)
    - CPU/Bridge for monitoring and control
    - TTC / Synchronization signal fanout
HCAL Trigger/Readout Card (HTR)

• All I/O on front panel
  – DAQ data output to DCC:
    • Single connector (LVDS) 16 bit x 40MHz
  – Timing Input (Encoded TTC, CLK, BC0):
    • Single connector (LVDS)
  – FE data Inputs:
    • 12-16 digital serial fibers from RBX
  – Level 1 Trigger Tower data outputs:
    • 8 shielded twisted pair
    • 4 per single 9-pin D connector

• FPGA logic implements:
  – Level 1 Path:
    • Trigger primitive preparation
    • Transmission to Level 1
  – Level 2/DAQ Path:
    • Buffering for Level 1 Decision
    • No filtering or crossing determination necessary
    • Transmission to DCC for Level 2/DAQ readout
HCAL Data Concentrator VME Module

Total of ~ 26 For all of HCAL

Encoded TTC (LVDS)

Level 1 and 2 Data from HTRs
1 event per L1A Per input
LVDS Channel Link 40MHz 16 bit
Total input bandwidth Limited to 200 Mbytes/s With current architecture

Level 2 Data to RUI S-Link 64 - 200 Mbytes/s expected average

Trigger Primitives To Trigger Data Conc. S-Link 32/64

Fast Overflow Warn (single NIM?)

Fast Busy Fast Ready (single NIMs?)
HCAL DCC Prototype Architecture

PC-MIP Mezzanine Cards
3 Channel Link Receivers

Data Concentrator Logic PMC

TTCRx

PCI
33/32

PCI-VME Bridge

S-Link (64) LSC

SDRAM

DCC FPGA

PCI
33/64

Overflow Warning
Fast Busy

To TTS

to RUI

to Trig
Data Conc.
3-Channel LVDS Receivers

33MHz PCI bus 1

33MHz PCI bus 2

33MHz PCI bus 3

PCI Bridge X

PCI Bridge Y

3.3V

5V

32

PMC Card (Standard)

Spare PMC Site

PMC Card (oversize)

DCC Logic Board

JTAG Test/Config

Local Control

64

PCI busses give access to all devices for monitoring

VME-PCI

Universe II

J3 VME Aux

Universe II VME-PCI

VME 64x

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PC-MIP 3 Channel Link Receiver

- 3 “Channel Link” LVDS receivers
- PCI target interface
- On-board logic:
  - ECC (Hamming)
    - Correct 1-bit, detect multi-bit
  - On-the-fly Event Building
  - Event number checking
  - Overflow warning (discard data payload on overflow)
  - Missing header/trailer detection & repair
  - Monitoring:
    - Count of words, events, errors
    - Status update on “marked” event for synchronization of monitoring
  - Status: 10 second-generation prototypes build (design is done)

![Diagram of PC-MIP 3 Channel Link Receiver](image)

- LVDS Serial Receivers (i.e. National Semi "Channel Link")
- SDRAM 2Mx32
- ALTERA (ACEX 1K130)
- PCI Bus (32 bit 33 MHz)
- FPGA (PCI Interface and readout/monitor logic)
- Event Fragments combined during PCI bus transfer
- Link Receiver Board(s)
- Logic Board
PC-MIP 3-Channel Link Receiver
DCC Logic Board

• Features:
  – On-board TTCrx controls operation
  – 3 Altera FPGAs for PCI interfaces (use Altera core)
  – Xilinx Virtex-2 contains all other logic:
    • Event Builder
    • Monitoring
    • Buffering (DDR SDRAM interface at 800Mbytes/s)
    • S-Link output (32 in demo; 64 final)
  – On-board flash memory for FPGA initialization
  – JTAG Interface

• Status:
  – Prototype PCB in Fab; free (!)
    XC2V1000 FPGAs in hand
  – Testing to begin in June ‘01
HCAL DAQ Buffering

HTR

- L1A
- 40MHz
- Derand. Buffer
- Link Tx
- Derand. Buffer
- Link Tx
- Derand. Buffer
- Link Tx

Derandomizer Buffer Protected against overflow by trigger rules

LVDS link speed same as HTR output logic → no bottleneck
[18 Links per DCC]

DCC

- 512kb FIFO
- >1000 events
- PCI
- 32/33
- Event Builder
- 8Mb Buffer
- > 4000 events

Link RX logic discards data when FIFO “almost full” (block structure maintained)

PCI 32/33

(2) 33MHz 32 bit PCI busses

~ 100MHz Processing

S-Link Interface

S-Link LSC

Busy/Ready

Overflow Warning

To TTS

Level 2 Data

To RUI

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HCAL Controls and Monitoring

• Fast Controls (via TTC):
  – L1A, Start Run, Stop Run
  – Reset (complete and partial – need to define!)

• Fast Monitoring (dedicated signals to TTS)
  – Overflow Warning (buffer full above preset limit)
  – Busy/Ready (reset, start/stop completed)

• Slow Monitoring (via CPU only)
  – All error conditions (link errors, loss of sync, etc)
• Run Control
  – Initialization, shutdown
  – “Slow” monitoring via VME
  – Error recovery:
    • Monitor status registers of modules via VME
    • Report serious errors via DCS
    • Reset/Restart on command

• TTC Fanout
  – Fanout encoded TTC, BC0, CLK to all modules
  – Needs I²C Control of local TTCrx
HCAL Timing / L1A Distribution

- Fanout Both:
  - Encoded TTC signal
    - For synchronization with incoming FE data (individual skew control)
  - Decoded BC0, CLK
    - For synchronization across all HCAL of TPG to Level 1
  - Details same as ECAL (J.C.DaSilva presentation)

**TTC Fanout (1 per crate)**

**HTR Cards**

- TTCrx
- Decode FPGA
- LVDS F/O
- PIN Diode

- BC0, CLK (TPG)
- BC0, CLK (FE)
HCAL DAQ Data Format

- Data format follows TriDAS Guidelines → → →
- HCAL payload: (details t.b.d)
  - Raw QIE (ADC) samples
  - Level 2 Filter output
  - Trigger Primitives
  - Zero-suppression mask
  - Error summary:
    - Front-end errors
    - Uncorrected Link errors
    - Synchronization errors
- We will stay tuned for updates to the data format → → →
HCAL Readout Status

- Front-End:
  - RBX Mechanics/Cooling Designed
  - Readout Card prototypes due Fall ‘01
- HTR:
  - 6U Demonstrator prototypes under test
- DCC:
  - 9U Demonstrator prototypes due in 2 weeks
  - No major changes anticipated for production version
- HRC:
  - Use commercial CPU for now
  - Need to design TTC fanout (ala ECAL)
- Major Concerns:
  - QIE Performance (pending prototype tests this summer)
  - Performance of 1.6 Gbit GOL link
  - System modularity (# channels per crate)
  - HF Front-End Packaging

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