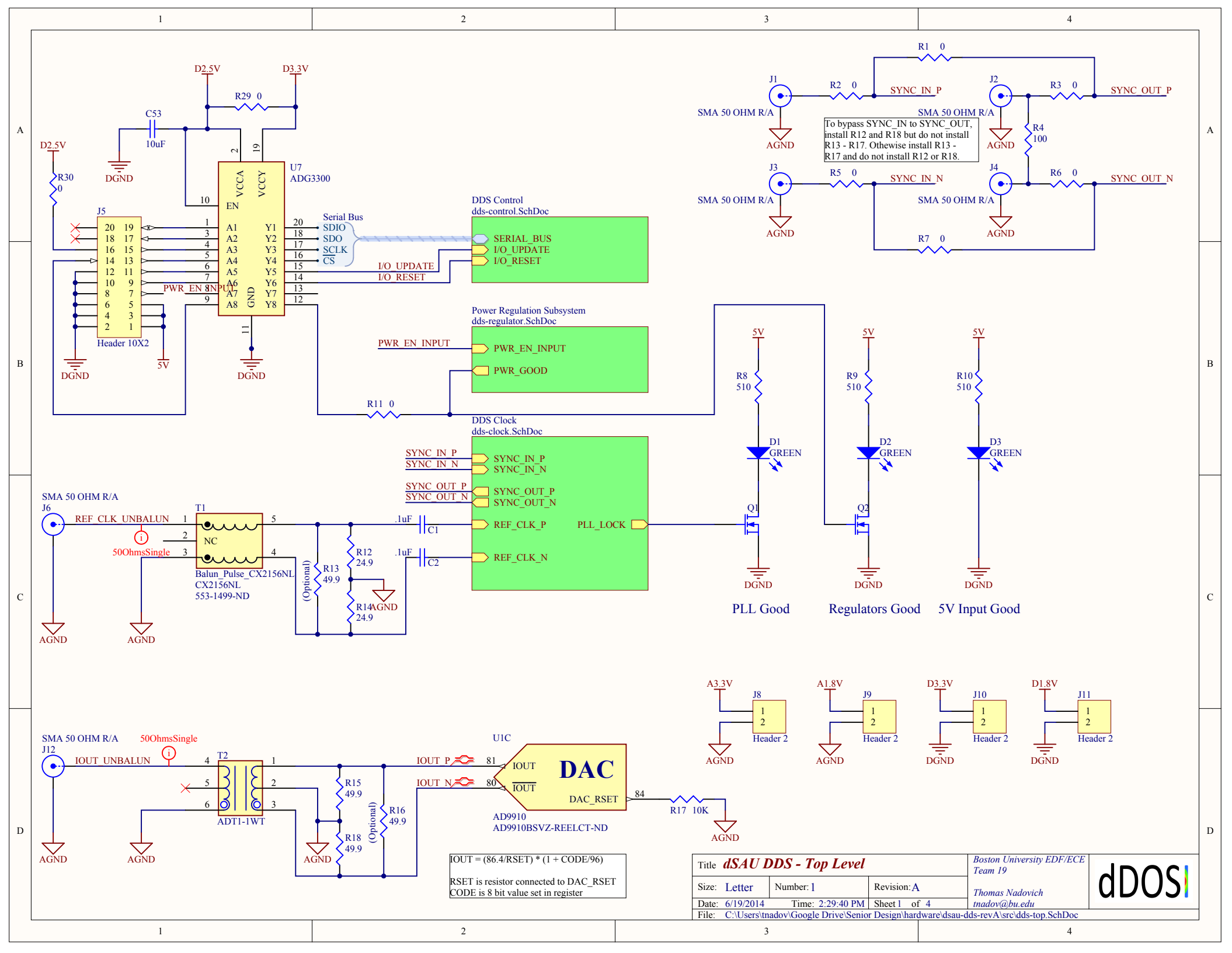
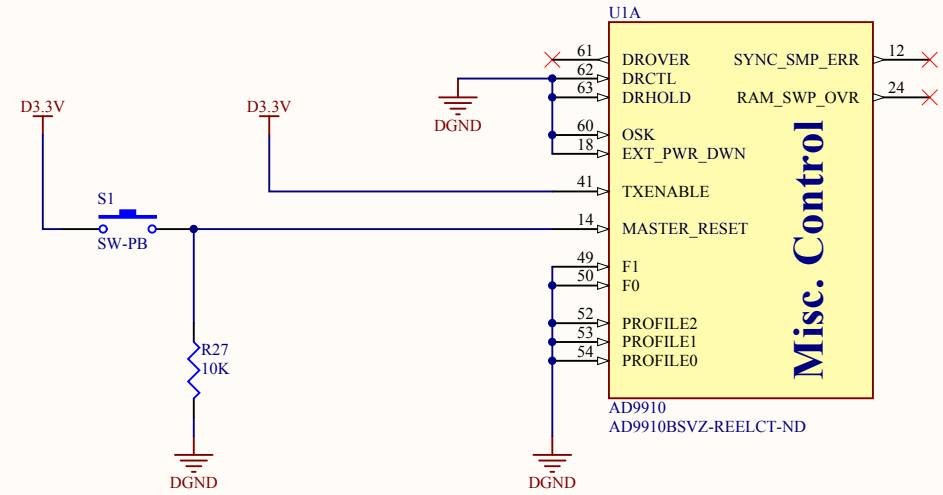
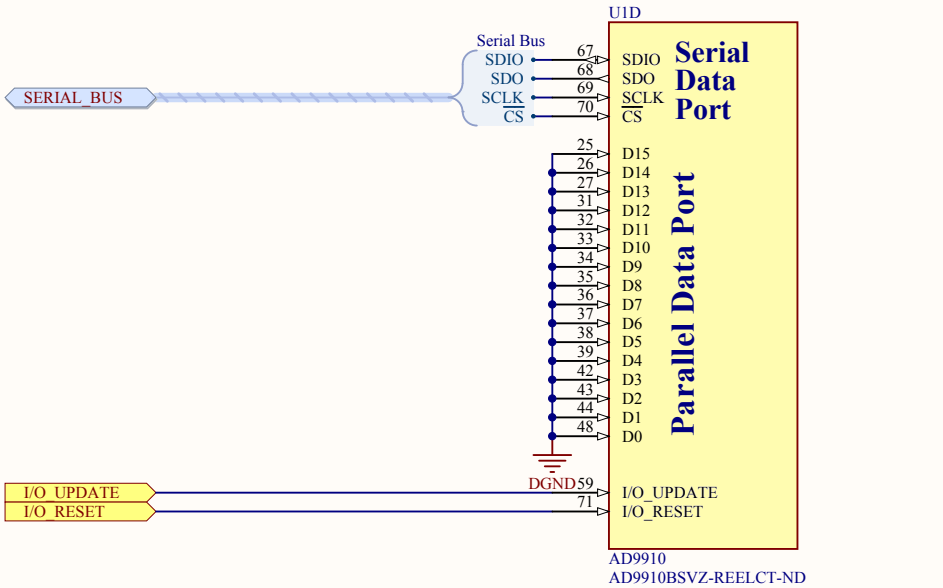

D2.5V
D3.3V
R29 0
C53
10uF
DGND
U7
ADG3300
VCCA
VCCY
EN
GND
A1
A2
A3
A4
A5
A6
A7
A8
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
R30
0
J5
Header 10X2
5V
Serial Bus
SDIO
SDO
SCLK
CS
DDS Control
dds-control.SchDoc
SERIAL_BUS
I/O_UPDATE
I/O_RESET
PWR_EN_INPUT
Power Regulation Subsystem
dds-regulator.SchDoc
PWR_GOOD
R11 0
DDS Clock
dds-clock.SchDoc
SYNC_IN_P
SYNC_IN_N
SYNC_OUT_P
SYNC_OUT_N
REF_CLK_P
REF_CLK_N
PLL_LOCK
R1 0
J1
J2
R2 0
R3 0
SYNC_IN_P
SYNC_OUT_P
SMA 50 OHM R/A
AGND
R4
100
To bypass SYNC_IN to SYNC_OUT, install R12 and R18 but do not install R13 - R17. Othewise install R13 - R17 and do not install R12 or R18.
J3
J4
R5 0
R6 0
SYNC_IN_N
SYNC_OUT_N
R7 0
5V
R8
510
R9
510
R10
510
D1
GREEN
D2
GREEN
D3
GREEN
Q1
Q2
PLL Good
Regulators Good
5V Input Good
J6
REF_CLK_UNBALUN
50OhmsSingle
T1
NC
Balun_Pulse_CX2156NL
CX2156NL
553-1499-ND
.1uF
C1
C2
R12
24.9
R13
49.9
(Optional)
R14
24.9
J12
IOUT_UNBALUN
T2
ADT1-1WT
R15
49.9
R16
49.9
R18
49.9
IOUT_P
IOUT_N
U1C
DAC
IOUT
IOUT
DAC_RSET
AD9910
AD9910BSVZ-REELCT-ND
R17 10K
A3.3V
A1.8V
D3.3V
D1.8V
J8
J9
J10
J11
Header 2
IOUT = (86.4/RSET) * (1 + CODE/96)
RSET is resistor connected to DAC_RSET
CODE is 8 bit value set in register
Title dSAU DDS - Top Level
Size: Letter
Number: 1
Revision: A
Date: 6/19/2014
Time: 2:29:40 PM
Sheet 1 of 4
File: C:\Users\tnadov\Google Drive\Senior Design\hardware\dsau-dds-revA\src\dds-top.SchDoc
Boston University EDF/ECE Team 19
Thomas Nadovich
tnadov@bu.edu
dDOSI





Title: *dSAU DDS - Control System*			*Boston University EDF/ECE Team 19*
Size: Letter	Number: 2	Revision: A	*Thomas Nadovich*
Date: 6/19/2014	Time: 2:29:40 PM	Sheet 2 of 4	*tnadov@bu.edu*
File: C:\Users\tnadov\Google Drive\Senior Design\hardware\dsau-dds-revA\src\dds-control.SchDoc			

dDOS

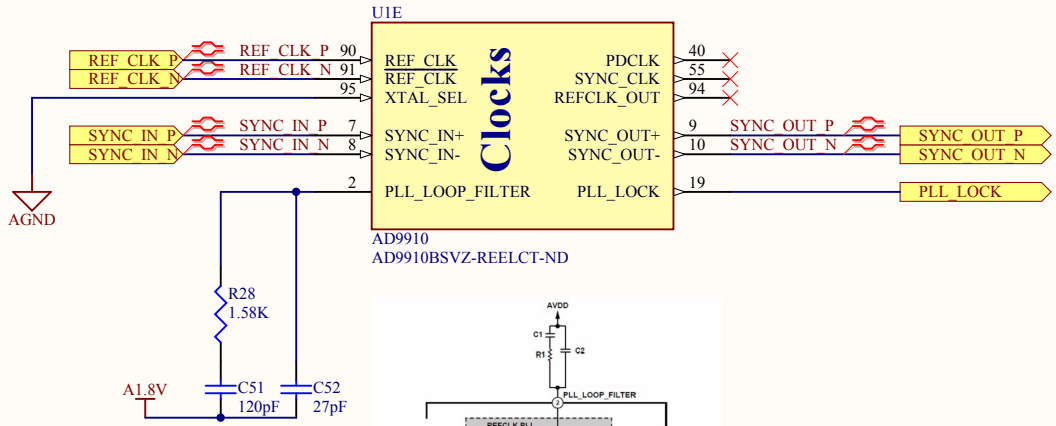


Figure 35. REFCLK PLL External Loop Filter

In the prevailing literature, this configuration yields a third-order, Type II PLL. To calculate the loop filter component values, begin with the feedback divider value (N), the gain of the phase detector (K_D), and the gain of the VCO (K_V) based on the programmed VCO SEL bit settings (see Table 1 for K_V). The loop filter component values depend on the desired open-loop bandwidth (f_{OL}) and phase margin (φ), as follows:

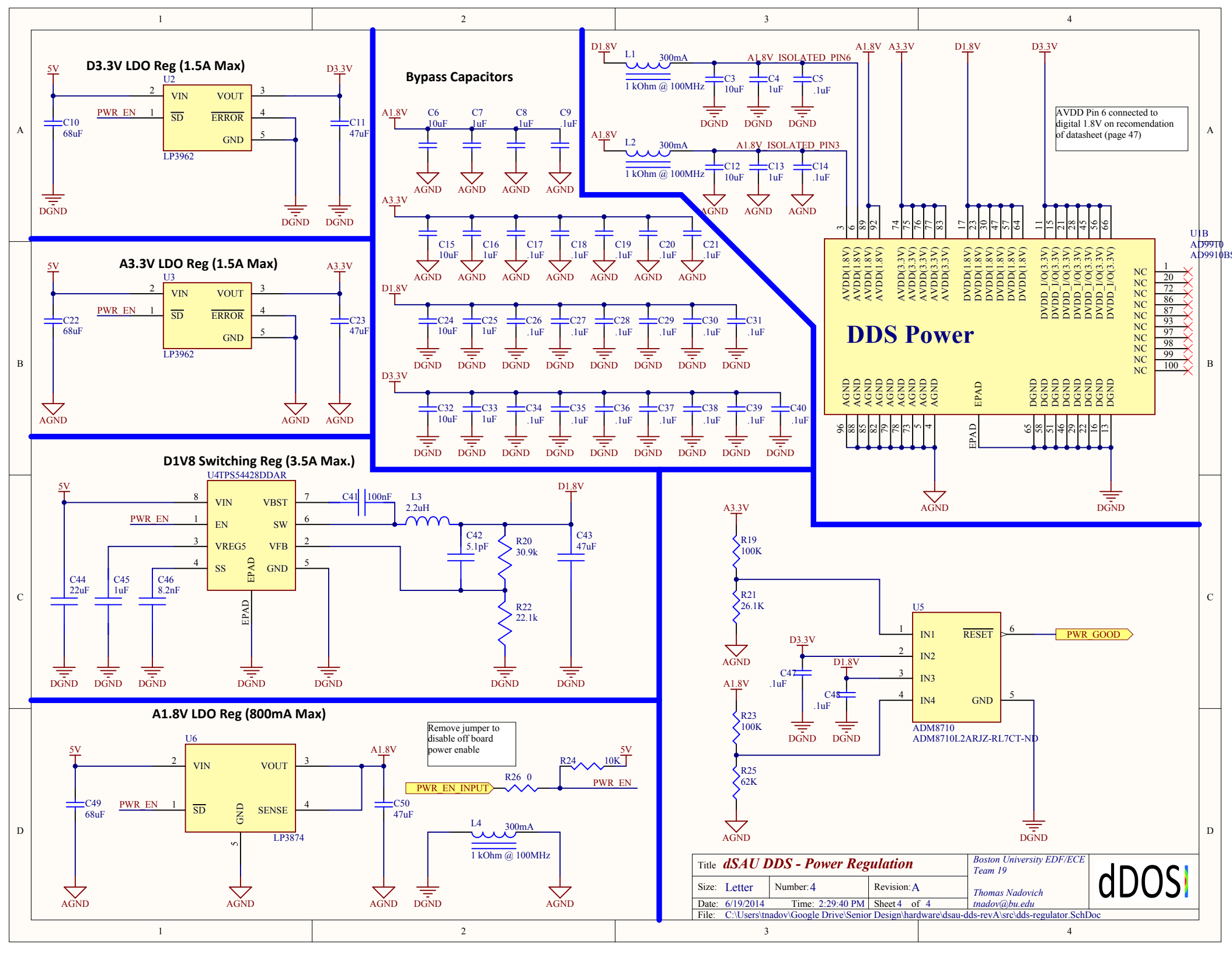
$$R1 = \frac{\pi N f_{OL}}{K_D K_V}\left(1+\frac{1}{\sin(\varphi)}\right) \quad (4)$$

$$C1 = \frac{K_D K_V \tan(\varphi)}{2N(\pi f_{OL})^2} \quad (5)$$

$$C2 = \frac{K_D K_V}{N(2\pi f_{OL})^2}\left(\frac{1-\sin(\varphi)}{\cos(\varphi)}\right) \quad (6)$$

Title	***dSAU DDS - Clocks & Synchronisation***		*Boston University EDF/ECE Team 19*
Size: Letter	Number: 3	Revision: A	*Thomas Nadovich*
Date: 6/19/2014	Time: 2:29:40 PM	Sheet 3 of 4	*tnadov@bu.edu*
File: C:\Users\tnadov\Google Drive\Senior Design\hardware\dsau-dds-revA\src\dds-clock.SchDoc			

dDOSI


D3.3V LDO Reg (1.5A Max)
A3.3V LDO Reg (1.5A Max)
D1V8 Switching Reg (3.5A Max.)
A1.8V LDO Reg (800mA Max)
Bypass Capacitors
DDS Power
AVDD Pin 6 connected to digital 1.8V on recomendation of datasheet (page 47)
Remove jumper to disable off board power enable
PWR_GOOD
PWR_EN_INPUT
ADM8710
ADM8710L2ARJZ-RL7CT-ND
LP3962
LP3874
U4TPS54428DDAR
Title dSAU DDS - Power Regulation
Boston University EDF/ECE Team 19
Thomas Nadovich
tnadov@bu.edu
Size: Letter
Number: 4
Revision: A
Date: 6/19/2014
Time: 2:29:40 PM
Sheet 4 of 4
File: C:\Users\tnadov\Google Drive\Senior Design\hardware\dsau-dds-revA\src\dds-regulator.SchDoc