The LT®1468 is a precision high speed operational amplifier with 16-bit accuracy and 900ns settling to 150µV for 10V signals. This unique blend of precision and AC performance makes the LT1468 the optimum choice for high accuracy applications such as DAC current-to-voltage conversion and ADC buffers. The initial accuracy and drift characteristics of the input offset voltage and inverting input bias current are tailored for inverting applications.

The 90MHz gain bandwidth ensures high open-loop gain at frequency for reducing distortion. In noninverting applications such as an ADC buffer, the low distortion and DC accuracy allow full 16-bit AC and DC performance.

The 22V/µs slew rate of the LT1468 improves large-signal performance in applications such as active filters and instrumentation amplifiers compared to other precision op amps.

The LT1468 is manufactured on Linear Technology’s complementary bipolar process.

LTC® and LT are registered trademarks of Linear Technology Corporation.
**ABSOLUTE MAXIMUM RATINGS**

(Noe 1)

- Total Supply Voltage ($V^+ \text{ to } V^-$) ...................... 36V
- Maximum Input Current (Note 2) ..................... 10mA
- Output Short-Circuit Duration (Note 3) ........ Indefinite
- Specified Temperature Range (Note 4) ... –40°C to 85°C
- Junction Temperature ................................... 150°C
- Storage Temperature Range ................... –65°C to 150°C
- Lead Temperature (Soldering, 10 sec) .......... 300°C

**PACKAGE/ORDER INFORMATION**

<table>
<thead>
<tr>
<th>ORDER PART NUMBER</th>
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<td>LT1468CN8</td>
<td>LT1468CS8</td>
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<tr>
<td>LT1468IN8</td>
<td>LT1468IS8</td>
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*S8 PART MARKING*

1468

1468I

Consult factory for Military Grade parts.

---

**ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ \text{C}, V_{CM} = 0\text{V}$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>$V_{SUPPLY}$</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<td>$V_{OS}$</td>
<td>Input Offset Voltage</td>
<td>$\pm 15\text{V}$</td>
<td>$\pm 5\text{V}$</td>
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<td>nA</td>
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<td>$I_{I}$</td>
<td>Inverting Input Bias Current</td>
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<td>10</td>
<td>nA</td>
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<td>Noninverting Input Bias Current</td>
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<td>40</td>
<td>nA</td>
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<td>Input Noise Voltage</td>
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<td>$\pm 5\text{V}$ to $\pm 15\text{V}$</td>
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<td>μV</td>
<td>μV</td>
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<td>$n_i$</td>
<td>Input Noise Voltage</td>
<td>$f = 10\text{kHz}$</td>
<td>$\pm 5\text{V}$ to $\pm 15\text{V}$</td>
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<td>$V_{CM} = \pm 12.5\text{V}$</td>
<td>$\pm 15\text{V}$</td>
<td>96</td>
<td>110</td>
<td>dB</td>
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<td>$PSRR$</td>
<td>Power Supply Rejection Ratio</td>
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<td>dB</td>
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<td>$A_{VOL}$</td>
<td>Large-Signal Voltage Gain</td>
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<td>dB</td>
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<td>mA</td>
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<td>Short-Circuit Current</td>
<td>$V_{OUT} = 0\text{V}, V_{IN} = \pm 0.2\text{V}$</td>
<td>$\pm 15\text{V}$</td>
<td>25</td>
<td>40</td>
<td>mA</td>
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## Electrical Characteristics

### SYMBOL | PARAMETER | CONDITIONS | \( V_{\text{SUPPLY}} \) | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | --- | ---
SR | Slew Rate | \( A_V = -1, R_L = 2k \) (Note 5) | ±15V | 15 | 22 | V/μs | μs/V
 | | | ±5V | 11 | 17 | |
GBW | Gain Bandwidth | \( f = 100kHz, R_L = 2k \) | ±15V | 60 | 90 | MHz | MHz
 | | | ±5V | 55 | 88 | |
THD | Total Harmonic Distortion | \( A_V = 2, V_O = 10V_{\text{P-P}} \) | ±15V | 0.00007 | 0.0015 | % |%
 | | | ±5V | 0.00007 | 0.0015 | % |%
\( t_r, t_f \) | Rise Time, Fall Time | \( A_V = 1 \), 10% to 90%, 0.1V | ±15V | 11 | 12 | ns | ns
 | | | ±5V | 30 | 35 | % |%
 | Overshoot | \( A_V = 1 \), 0.1V | ±15V | 9 | 10 | ns | ns
 | | | ±5V | 11 | 12 | ns | ns
\( t_s \) | Settling Time | 10V Step, 0.01%, \( A_V = -1 \) | ±15V | 760 | 900 | ns | ns
 | | | ±5V | 770 | 900 | ns | ns
\( R_O \) | Output Resistance | \( A_V = 1 \), \( f = 100kHz \) | ±15V | 0.02 | 0.03 | Ω | Ω
\( I_S \) | Supply Current | | ±15V | 3.9 | 5.2 | mA | mA
### \( 0^\circ C \leq T_A \leq 70^\circ C, V_{CM} = 0V \) unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | \( V_{\text{SUPPLY}} \) | MIN | TYP | MAX | UNITS
--- | --- | --- | --- | --- | --- | --- | ---
\( V_{DS} \) | Input Offset Voltage | ±15V | ● | 150 | μV | μV
 | | ±5V | ● | 250 | μV | μV
\( I_{ODS} \) | Input Offset Current | ±5V to ±15V | ● | 0.7 | 2.0 | μA/°C | μA/°C
\( I_{OS} \) | Input Offset Current Drift | ±5V to ±15V | ● | 65 | nA | nA
\( I_{B^-} \) | Inverting Input Bias Current | ±5V to ±15V | ● | ±15 | nA | nA
\( I_{B^+} \) | Noninverting Input Bias Current | ±5V to ±15V | ● | ±50 | nA | nA
CMRR | Common Mode Rejection Ratio | \( V_{CM} = ±12.5V \) | ±15V | 94 | 94 | dB | dB
 | | \( V_{CM} = ±2.5V \) | ±5V | 94 | 94 | dB | dB
PSRR | Power Supply Rejection Ratio | \( V_S = ±4.5V \) to ±15V | ● | 98 | dB | dB
\( A_{VOL} \) | Large-Signal Voltage Gain | \( V_{OUT} = ±12.5V, R_L = 10k \) | ±15V | 500 | V/mV | V/mV
 | | \( V_{OUT} = ±12.5V, R_L = 2k \) | ±15V | 250 | V/mV | V/mV
 | | \( V_{OUT} = ±2.5V, R_L = 10k \) | ±5V | 500 | V/mV | V/mV
 | | \( V_{OUT} = ±2.5V, R_L = 2k \) | ±5V | 250 | V/mV | V/mV
\( V_{OUT} \) | Output Swing | \( R_L = 10k \) | ±15V | ±12.9 | V | V
 | | \( R_L = 2k \) | ±15V | ±12.7 | V | V
 | | \( R_L = 10k \) | ±5V | ±2.9 | V | V
 | | \( R_L = 2k \) | ±5V | ±2.7 | V | V
\( I_{OUT} \) | Output Current | \( V_{OUT} = ±12.5V \) | ±15V | ±12.5 | mA | mA
 | | \( V_{OUT} = ±2.5V \) | ±5V | ±12.5 | mA | mA
\( I_{SC} \) | Short-Circuit Current | \( V_{OUT} = 0V, V_{IN} = ±0.2V \) | ±15V | ±17 | mA | mA
SR | Slew Rate | \( A_V = -1, R_L = 2k \) (Note 5) | ±15V | 13 | 9 | V/μs | V/μs

\( T_A = 25^\circ C, V_{CM} = 0V \) unless otherwise noted.
## ELECTRICAL CHARACTERISTICS

$0^\circ C \leq T_A \leq 70^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

### SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS
---|---|---|---|---|---|---|---
$\text{GBW}$ | Gain Bandwidth | $f = 100kHz$, $R_L = 2k$ | $\pm15V$ | ● | 55 | ● | MHz
 | | | $\pm5V$ | ● | 50 | | MHz
$I_S$ | Supply Current | | $\pm15V$ | ● | 6.5 | | mA
 | | | $\pm5V$ | ● | 6.3 | | mA

$-40^\circ C \leq T_A \leq 85^\circ C$, $V_{CM} = 0V$ unless otherwise noted (Note 4).

### SYMBOL | PARAMETER | CONDITIONS | $V_{SUPPLY}$ | MIN | TYP | MAX | UNITS
---|---|---|---|---|---|---|---
$V_{OS}$ | Input Offset Voltage | | $\pm15V$ | ● | 230 | | $\mu V$
 | | | $\pm5V$ | ● | 330 | | $\mu V$
 | Input $V_{OS}$ Drift | (Note 7) | $\pm5V$ to $\pm15V$ | ● | 0.7 | | $\mu V/^\circ C$
$I_{OS}$ | Input Offset Current | | $\pm5V$ to $\pm15V$ | ● | 80 | | nA
 | Input Offset Current Drift | | $\pm5V$ to $\pm15V$ | | 120 | | $pA/^\circ C$
$I_g^-$ | Inverting Input Bias Current | | $\pm5V$ to $\pm15V$ | ● | ±30 | | nA
 | Noninverting Input Bias Current | | $\pm5V$ to $\pm15V$ | ● | ±60 | | nA
CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm12.5V$ | $\pm15V$ | ● | 92 | | dB
 | | $V_{CM} = \pm2.5V$ | $\pm5V$ | ● | 92 | | dB
PSRR | Power Supply Rejection Ratio | $V_S = \pm4.5V$ to $\pm15V$ | | | 96 | | dB
$A_{VOL}$ | Large-Signal Voltage Gain | $V_{OUT} = \pm12V$, $R_L = 10k$ | $\pm15V$ | ● | 300 | | V/mV
 | | $V_{OUT} = \pm10V$, $R_L = 2k$ | $\pm15V$ | ● | 150 | | V/mV
 | | $V_{OUT} = \pm2.5V$, $R_L = 10k$ | $\pm5V$ | ● | 300 | | V/mV
 | | $V_{OUT} = \pm2.5V$, $R_L = 2k$ | $\pm5V$ | ● | 150 | | V/mV
$V_{OUT}$ | Output Swing | $R_L = 10k$ | $\pm15V$ | ● | ±12.8 | | V
 | $R_L = 2k$ | $\pm15V$ | ● | ±12.6 | | V
 | $R_L = 10k$ | $\pm5V$ | ● | ±2.8 | | V
 | $R_L = 2k$ | $\pm5V$ | ● | ±2.6 | | V
$I_{OUT}$ | Output Current | $V_{OUT} = \pm12.5V$ | $\pm15V$ | ● | ±7 | | mA
 | $V_{OUT} = \pm2.5V$ | $\pm5V$ | ● | ±7 | | mA
$I_{SC}$ | Short-Circuit Current | $V_{OUT} = 0V$, $V_{IN} = \pm0.2V$ | $\pm15V$ | ● | ±12 | | mA
SR | Slew Rate | $A_V = -1$, $R_L = 2k$ (Note 5) | $\pm15V$ | ● | 9 | | $V/\mu s$
 | | $\pm5V$ | ● | 6 | | $V/\mu s$
GBW | Gain Bandwidth | $f = 100kHz$, $R_L = 2k$ | $\pm15V$ | ● | 45 | | MHz
 | | $\pm5V$ | ● | 40 | | MHz
$I_S$ | Supply Current | | $\pm15V$ | ● | 7.0 | | mA
 | | $\pm5V$ | ● | 6.8 | | mA

The ● denotes specifications that apply over the full operating temperature range.

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The inputs are protected by back-to-back diodes and two 100Ω series resistors. If the differential input voltage exceeds 0.7V, the input current should be limited to 10mA. Input voltages outside the supplies will be clamped by ESD protection devices and input currents should also be limited to 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

**Note 4:** The LT1468C is guaranteed to meet specified performance from $0^\circ C$ to $70^\circ C$ and is designed, characterized and expected to meet these extended temperature limits, but is not tested at $-40^\circ C$ and at $85^\circ C$. The LT1468I is guaranteed to meet the extended temperature limits.

**Note 5:** Slew rate is measured between $-8V$ on the output with $-12V$ input for $-15V$ supplies and $-2V$ on the output with $-3V$ input for $-5V$ supplies.

**Note 6:** Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\sqrt{VP}$

**Note 7:** This parameter is not 100% tested.
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature

Input Common Mode Range vs Supply Voltage

Input Bias Current vs Input Common Mode Voltage

Input Bias Current vs Temperature

Input Noise Spectral Density

0.1Hz to 10Hz Voltage Noise

Warm-Up Drift vs Time

Open-Loop Gain vs Resistive Load

Open-Loop Gain vs Temperature
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Output Voltage Swing vs Supply Voltage**

![Graph showing output voltage swing vs supply voltage with labels and parameters]

**Output Voltage Swing vs Load Current**

![Graph showing output voltage swing vs load current with labels and parameters]

**Output Short-Circuit Current vs Temperature**

![Graph showing output short-circuit current vs temperature with labels and parameters]

**Settling Time to 0.01% vs Output Step, $V_S = \pm 15V$**

![Graph showing settling time vs output step with labels and parameters]

**Settling Time to 0.01% vs Output Step, $V_S = \pm 5V$**

![Graph showing settling time vs output step with labels and parameters]

**Settling Time to 150μV vs Output Step**

![Graph showing settling time vs output step with labels and parameters]

**Gain Bandwidth and Phase Margin vs Supply Voltage**

![Graph showing gain bandwidth and phase margin vs supply voltage with labels and parameters]

**Gain Bandwidth and Phase Margin vs Temperature**

![Graph showing gain bandwidth and phase margin vs temperature with labels and parameters]

**Output Impedance vs Frequency**

![Graph showing output impedance vs frequency with labels and parameters]
LT1468

**TYPICAL PERFORMANCE CHARACTERISTICS**

![Diagram showing Total Harmonic Distortion + Noise vs Frequency](image1)

- **Total Harmonic Distortion + Noise vs Frequency:**
  - $V_S = \pm 15V$
  - $T_A = 25^\circ C$
  - $R_L = 600\Omega$
  - $V_D = 20V_{p-p}$
  - NOISE BW = 80kHz

![Diagram showing Total Harmonic Distortion + Noise vs Amplitude](image2)

- **Total Harmonic Distortion + Noise vs Amplitude:**
  - $T_A = 25^\circ C$
  - $A_V = 10$
  - $R_L = 600\Omega$
  - $f = 10kHz$
  - NOISE BW = 80kHz

![Diagram showing Undistorted Output Swing vs Frequency, $\pm 15V$](image3)

- **Undistorted Output Swing vs Frequency, $\pm 15V$:**
  - $V_S = \pm 15V$
  - $R_L = 2k$

![Diagram showing Undistorted Output Swing vs Frequency, $\pm 5V$](image4)

- **Undistorted Output Swing vs Frequency, $\pm 5V$:**
  - $V_S = \pm 5V$
  - $R_L = 2k$

![Diagram showing Small-Signal Transient, $A_V = 1$](image5)

- **Small-Signal Transient, $A_V = 1$:**
  - $V_S = \pm 15V$

![Diagram showing Small-Signal Transient, $A_V = -1$](image6)

- **Small-Signal Transient, $A_V = -1$:**
  - $V_S = \pm 15V$

![Diagram showing Large-Signal Transient, $A_V = 1$](image7)

- **Large-Signal Transient, $A_V = 1$:**
  - $V_S = \pm 15V$

![Diagram showing Large-Signal Transient, $A_V = -1$](image8)

- **Large-Signal Transient, $A_V = -1$:**
  - $V_S = \pm 15V$

![Diagram showing Total Noise vs Unmatched Source Resistance](image9)

- **Total Noise vs Unmatched Source Resistance:**
  - $V_S = \pm 15V$
  - $T_A = 25^\circ C$
  - $f = 10kHz$
  - $R_L = 600\Omega$
APPLICATIONS INFORMATION

The LT1468 may be inserted directly into many operational amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1468 is shown below.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of the value:

$$C_F > \frac{(R_G)(C_{IN}/R_F)}{1}$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, $C_F$ should be greater than or equal to $C_{IN}$. An example would be a DAC I-to-V converter as shown on the front page of this data sheet where the DAC can have many tens of pF of output capacitance. Another example would be a gain of –1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor. The frequency response in a gain of –1 is shown in the Typical Performance curves with 2k and 5.1k resistors with a 5pF feedback capacitor.

Layout and Passive Components

The LT1468 requires attention to detail in board layout in order to maximize DC and AC performance. For best AC results (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01μF to 0.1μF) in parallel with low ESR bypass capacitors (1μF to 10μF tantalum). For best DC performance, use “star” grounding techniques, equalize input trace lengths and minimize leakage (i.e., 1.5GΩ of leakage between an input and a 15V supply will generate 10nA—equal to the maximum I8– specification.)

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs. For inverting configurations tie the ring to ground, in noninverting connections tie the ring to the inverting input (note the input capacitance will increase which may require a compensating capacitor as discussed below.)

Microvolt level error voltages can also be generated in the external circuitry. Thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the inputs can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Make no connection to Pin 8. This pin is used for factory trim of the inverting input current.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause peaking or even oscillations. For feedback resistors greater than 2k, a feedback capacitor of the value:

$$C_F > \frac{(R_G)(C_{IN}/R_F)}{1}$$

should be used to cancel the input pole and optimize dynamic performance. For applications where the DC noise gain is one, and a large feedback resistor is used, $C_F$ should be greater than or equal to $C_{IN}$. An example would be a DAC I-to-V converter as shown on the front page of this data sheet where the DAC can have many tens of pF of output capacitance. Another example would be a gain of –1 with 5k resistors; a 5pF to 10pF capacitor should be added across the feedback resistor. The frequency response in a gain of –1 is shown in the Typical Performance curves with 2k and 5.1k resistors with a 5pF feedback capacitor.

Nulling Input Capacitance

Input Considerations

Each input of the LT1468 is protected with a 100Ω series resistor and back-to-back diodes across the bases of the input devices. If the inputs can be pulled apart, the input current should be limited to less than 10mA with an external series resistor. Each input also has two ESD clamp diodes—one to each supply. If an input is driven above the supply, limit the current with an external resistor to less than 10mA.

The LT1468 employs bias current cancellation at the inputs. The inverting input current is trimmed at zero common mode voltage to minimize errors in inverting applications such as I-to-V converters. The noninverting input current is not trimmed and has a wider variation and therefore a larger maximum value. As the input offset
current can be greater than either input current, the use of balanced source resistance is NOT recommended as it actually degrades DC accuracy and also increases noise.

The input bias currents vary with common mode voltage as shown in the Typical Performance Characteristics. The cancellation circuit was not designed to track this common mode voltage because the settling time would have been adversely affected.

The LT1468 inputs can be driven to the negative supply and to within 0.5V of the positive supply without phase reversal. As the input moves closer than 0.5V to the positive supply, the output reverses phase.

Driving Capacitive Loads

\[
\begin{align*}
R_F & \geq (1 + R_f/R_G)/(2\pi C_L 5 \text{MHz}) \quad \text{for} \quad f > 10R_f/R_G \\
C_F & = (2R_O/R_F)C_L
\end{align*}
\]

Excellent Linear Technology reference sources for settling measurements, Application Notes 47 and 74. Appendix B of AN47 is a vital primer on 12-bit settling measurements, and AN74 extends the state of the art while concentrating on settling time with a 16-bit current output DAC input.

The 150μV settling curve in the Typical Performance Characteristics is measured using the Differential Amplifier method of AN74 followed by a clamped, nonsaturating gain of 100. The total gain of 500 allows a resolution of 100μV/DIV with an oscilloscope setting of 0.05V/DIV.

The settling of the DAC I-to-V converter on the front page was measured using the exact methods of AN74. The optimum nulling of the DAC output capacitance requires 20pF across the 6k feedback resistor. The theoretical limit for 16-bit settling is 11.1 times this RC time constant or 1.33μs. The actual settling time is 1.7μs at the output of the LT1468. The LT1468 is the fastest Linear Technology amplifier in this application.

The optional noise filter adds a slight delay of 100ns, but reduces the noise bandwidth to 1.6MHz which increases the output resolution for 16-bit accuracy.

Distortion

The LT1468 has outstanding distortion performance as shown in the Typical Performance curves of Total Harmonic Distortion + Noise vs Frequency and Amplitude. The high open-loop gain and inherently balanced architecture reduce errors to yield 16-bit accuracy to frequencies as high as 100kHz. An example of this performance is the Typical Application titled 100kHz Low Distortion Bandpass Filter. This circuit is useful for cleaning up the output of a high performance signal generator such as the B & K type 1051 or HP3326A.
Another key application for LT1468 is buffering the input to a 16-bit A/D converter. In a gain of 1 or 2, this straightforward circuit provides uncorrupted AC and DC levels to the converter, while buffering the A/D input sample-and-hold circuit from high source impedance which can reduce the maximum sampling rate. The front-page graph shows better than 16-bit distortion for a gain of 2 with a 10Vp-p output.

**Simplified Schematic**

**Package Description**

Dimensions in inches (millimeters) unless otherwise noted.

**N8 Package**
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

**S8 Package**
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

*These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.254mm).

*Dimension does not include mold flash. Mold flash shall not exceed 0.006 inch (0.152mm) per side.

**Dimension does not include interlead flash. Interlead flash shall not exceed 0.019 inch (0.49mm) per side.
### LT1468

#### TYPICAL APPLICATIONS

**Instrumentation Amplifier**

![Instrumentation Amplifier Circuit](image)

GAIN = \( \frac{R4}{R3} \left[ 1 + \frac{1}{2} \left( \frac{R2}{R1} + \frac{R3}{R4} \right) + \frac{R2 + R3}{R5} \right] \)

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION

**16-Bit ADC Buffer**

![16-Bit ADC Buffer Circuit](image)

**100kHz Low Distortion Bandpass Filter**

![100kHz Bandpass Filter Circuit](image)

**100kHz Distortion**

<table>
<thead>
<tr>
<th>SIGNAL LEVEL</th>
<th>RL</th>
<th>2ND HARMONIC</th>
<th>3RD HARMONIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1VRMS</td>
<td>1M</td>
<td>–106dB</td>
<td>–103dB</td>
</tr>
<tr>
<td>2VRMS</td>
<td>1M</td>
<td>–104dB</td>
<td>–104dB</td>
</tr>
<tr>
<td>3.5VRMS</td>
<td>1M</td>
<td>–103dB</td>
<td>–103dB</td>
</tr>
<tr>
<td>1VRMS</td>
<td>2k</td>
<td>–99dB</td>
<td>–103dB</td>
</tr>
<tr>
<td>2VRMS</td>
<td>2k</td>
<td>–96.5dB</td>
<td>–102dB</td>
</tr>
<tr>
<td>3.5VRMS</td>
<td>2k</td>
<td>–96.5dB</td>
<td>–102dB</td>
</tr>
</tbody>
</table>

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT1167</td>
<td>Precision Instrumentation Amplifier</td>
<td>Single Resistor Gain Set, 0.04% Max Gain Error, 10ppm Max Gain Nonlinearity</td>
</tr>
<tr>
<td>LTC1595/LTC1596</td>
<td>16-Bit Serial Multiplying I_OUT DACs</td>
<td>±1LSB Max INL/DNL, Low Glitch, DAC8043 16-Bit Upgrade</td>
</tr>
<tr>
<td>LTC1597</td>
<td>16-Bit Parallel Multiplying I_OUT DAC</td>
<td>±1LSB Max INL/DNL, Low Glitch, On-Chip Bipolar Resistors</td>
</tr>
<tr>
<td>LTC1604</td>
<td>16-Bit, 333ksps Sampling ADC</td>
<td>±2.5V Input, SINAD = 90dB, THD = –100dB</td>
</tr>
<tr>
<td>LTC1605</td>
<td>Single 5V, 16-Bit, 100ksps Sampling ADC</td>
<td>Low Power, ±10V Inputs, Parallel/Byte Interface</td>
</tr>
</tbody>
</table>