Control Registers in the Bio-Sensor FPGA

William E. Earle

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This document describes the 19 registers used to control the operation of the bio-sensor FPGA, or, more specifically, the part of the logic in the FPGA that communicates with the bio-sensor so as to collect and process sensor data. Most of the registers hold operating parameters such as the various bias voltages, with a few others used to supply processed readout data.

Before discussing the details of the control registers, it is helpful to provide a brief description of the bio-sensor as it relates to the FPGA logic, starting with the block diagram of Fig.1. The bio-sensor itself consists of eight specially constructed FET transistors, divided into two groups of four each, one group called the sample FET's and the other the reference FET's. The sample FET's are immersed in a sample solution that also contains a solution electrode. Similarly, the reference FET's are immersed in a reference solution that also contains a solution electrode.

As shown in Fig.1, the four drains of the sample FET's are connected together and driven by a signal called sample_drive, consisting of a dc bias, called sample_bias, plus a small ac signal. The four drains of the reference FET's are also connected together and driven by a signal called reference_drive, consisting of a dc bias, called reference_bias, plus the same ac signal used by the sample FET's.

The sources of all of the FET's are connected to individual selectable-gain transimpedance amplifiers that convert the source currents into voltage signals which feed the analog input circuit shown in block form in Fig.2.

Fig. 2 shows multiplexers that select one of the four sample transimpedance signals and one of the four reference transimpedance signals. These signals are summed with dc sample_offset and reference_offset signals and then amplified by gains of 100 before being sent to an A/D converter. The A/D

converter has an input multiplexer that selects either a sample signal (input A) or a reference signal (input B).

1 The 19 Registers

The data formats for the registers are shown in Fig. 3. The following describes the operation of the registers:

- A_D INPUT: This register controls the selection of the signals to the A/D converter. As the FPGA processes and stores bio-sensor data, A/D conversions alternate between an A input and a B input as specified by this register. The B input is simple, it allows for one of the four reference FET's or a test 1 Megohm resistor to be selected.

  The A input allows the selection of one of the four sample FET's or a 1 Megohm test resistor, but it also allows for four differential inputs. The differential inputs cause the A/D to convert the difference between the selected sample FET and the selected reference FET, or $SAMPLE - REFERENCE$.

- SAMPLE_BIAS: Writing to this register causes a serial data stream to be sent to a DAC that provides the DC sample bias. The value ranges from -2.5V to +2.5V. While the serial data is being sent to the DAC, the "serial_busy" bit in the COMMAND/STATUS register remains high. The relationship between the voltage and the register contents (in integer 2's complement format) is $REGISTER = VOLTAGE * 819.2$. For example to set the voltage to -1V, the register should contain -819.2, which is CCD (hex).

- REFERENCE_BIAS: Same as SAMPLE_BIAS, but provides the reference bias.

- SAMPLE_SOLUTION: Same as SAMPLE_BIAS but drives the sample solution electrode.

- REFERENCE_SOLUTION: Same as SAMPLE_BIAS but drives the reference solution electrode.

- SAMPLE_OFFSET: Similar to SAMPLE_BIAS but has a range of -1.024V to +1.024V. Used to remove most of the DC component from

the A input to the A/D. May be written directly, but normally is set by the zero command. After a "zero" operation, the value of SAMPLE_OFFSET is a measure of the DC current through the sample FET. When $G = 1$, $\mu amps = REGISTER/2000$, or when $G = 0.1$, $\mu amps = REGISTER/200$.

- REFERENCE_OFFSET: Same as SAMPLE_OFFSET but removes the dc component from the B input.

- A_OUT_INPHASE: This is a read-only register that is updated at the end of each cycle of the AC sinewave signal. It contains the amplitude of the AC in-phase component from the A input. In $\mu amps$ this current is given by $\mu amps = REGISTER/1,310,100$ for $G = 1$, or $\mu amps = REGISTER/131,010.1$ for $G = 0.1$.

- A_OUT_QUADRATURE: Same as A_OUT_INPHASE but contains the quadrature component from the A input.

- B_OUT_INPHASE: Same as A_OUT_INPHASE but contains the in-phase component from the B input.

- B_OUT_QUADRATURE: Same as B_OUT_INPHASE but contains the quadrature component from the B input.

- A_RAW_DATA: This is a FIFO-like read-only register that contains raw A/D data from the A input over one cycle of the ac sinewave signal (256 values). The values in this register are only updated after a save_one_cycle command is executed. Normally this register is only used for system test and trouble-shooting. 256 reads of this register are needed to return the data for one complete AC drive cycle.

- B_RAW_DATA: Same as A_RAW_DATA but contains data from the B input.

- PHASE_INCREMENT_L: The lower 16 bits of the 22 bit phase increment that determines the frequency of the AC sinewave. PHASE_INCREMENT_H contains the upper six bits. A value of 2,199,023 (218DEF hex) will set the frequency to 100 Hz and a value of 21,990 will give a 1 Hz frequency. For 17 Hz, the value would be 17/100 times 2,199,023, or 373,834. The maximum frequency is 190.7 Hz and the minimum frequency is about 0.75 Hz.

- COMMAND/STATUS: A one written to the zero bit causes the SAMPLE_OFFSET and REFERENCE_OFFSET values to be adjusted so as to set the DC levels of the A and B inputs as close as possible to midscale (1.25V). The AC drive signal is turned off during this zeroing operation. The zeroing operation requires one cycle of the AC drive signal, and its completion is indicated by the zero bit being read as a 0. After zeroing, the values in the A_A/D and B_A/D registers should be about 8000 hex. If the DC current exceeds $1\mu amp$ when $G = 1$ or $10\mu amps$ when $G = 0.1$ then the MAXIMUM_SAMPLE_OFFSET and/or the MAXIMUM_REFERENCE_OFFSET bits will be set, indicating that the zeroing operation was unsuccessful.

  A one written to the save bit causes one cycle of the A and B inputs (256 values each) to be saved in the A_RAW_DATA and B_RAW_DATA registers (pseudo FIFO's).

  The cycle_done bit is a symmetrical square wave with the rising-edge indicating new data in the INPHASE and QUADRATURE registers. When this signal goes high, the VALID bit should also be high. A zero VALID bit indicates that the INPHASE and QUADRATURE registers do not contain "clean" data because one or more control parameters were changed during the course of the AC drive cycle. The SAMPLE_A/D_OVERLOAD and REFERENCE_A/D_OVERLOAD bits should also be low when cycle_done goes high or the A/D was overdriven sometime during the AC drive cycle and the INPHASE and QUADRATURE registers do not contain correct data.

  There is also a serial_busy bit that shows when serial data is being sent to a DAC. Writing to a DAC register will only be successful when this bit is low.

  Two other bits, A_A/D_VALID and B_A/D_VALID, are provided to indicate when registers A_A/D and B_A/D contain valid data. If the SAMPLE_OFFSET or REFERENCE_OFFSET registers are written with new data, the A_A/D and B_A/D registers will not reflect the result of the changes until these two bits return high. These two VALID bits are mainly useful if one does not use the internal zeroing operation and wishes to do the zeroing by manually writing to the OFFSET registers.

- A_A/D: This is a read-only register that contains the most recent A/D

data from the A channel. This register is useful when debugging or for zeroing the A/D when the internal zeroing function is not used. This register is updated 256 times for each AC drive cycle; with a 100 Hz drive frequency, the update rate would be 25.6 kHz, or with a 1 Hz drive frequency, the update rate would be 256 Hz.

- B_ A/D: Same as A_A/D but for the B channel.
- VERSION: A read-only register containing the bio1.VHD version as a binary number. The version starts with 1 and is incremented each time the VHDL code is updated.

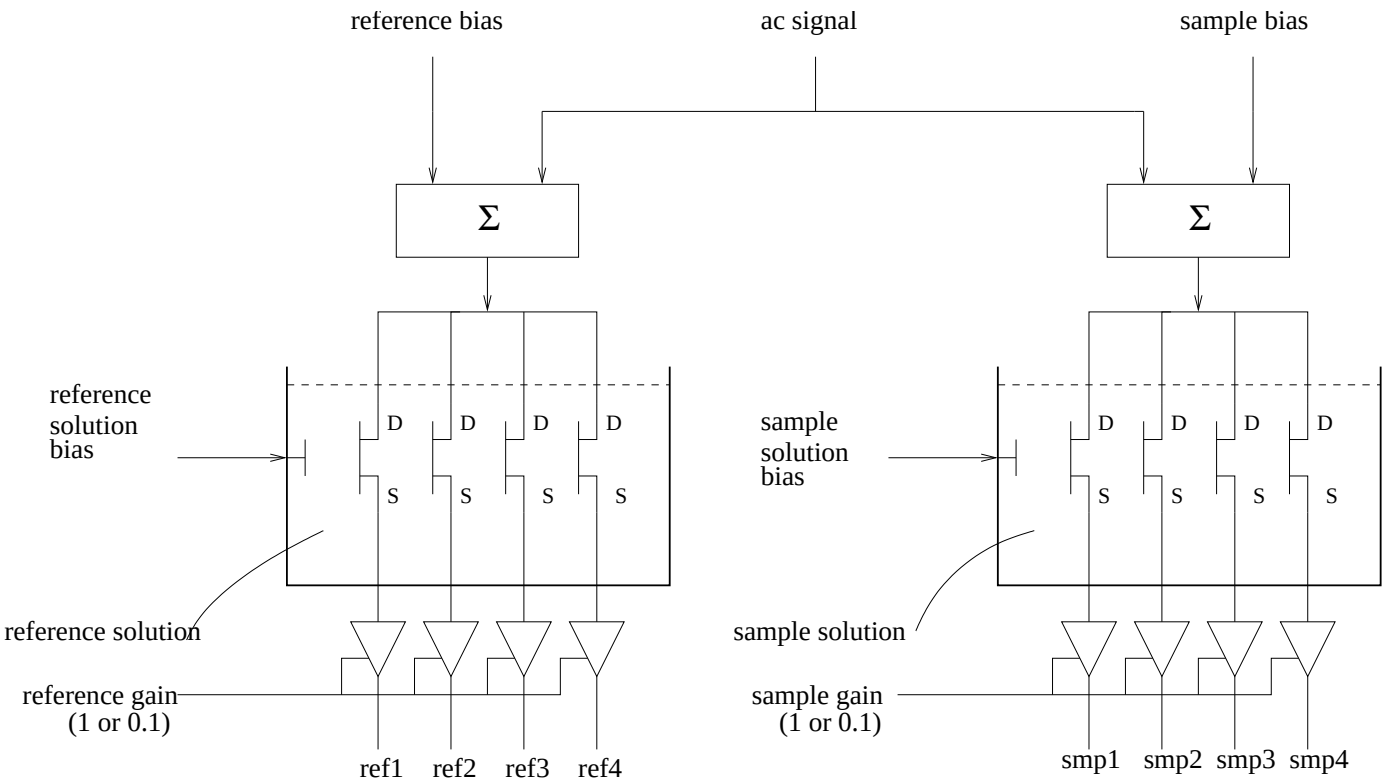

Fig. 1 Bio−sensor electrical connections

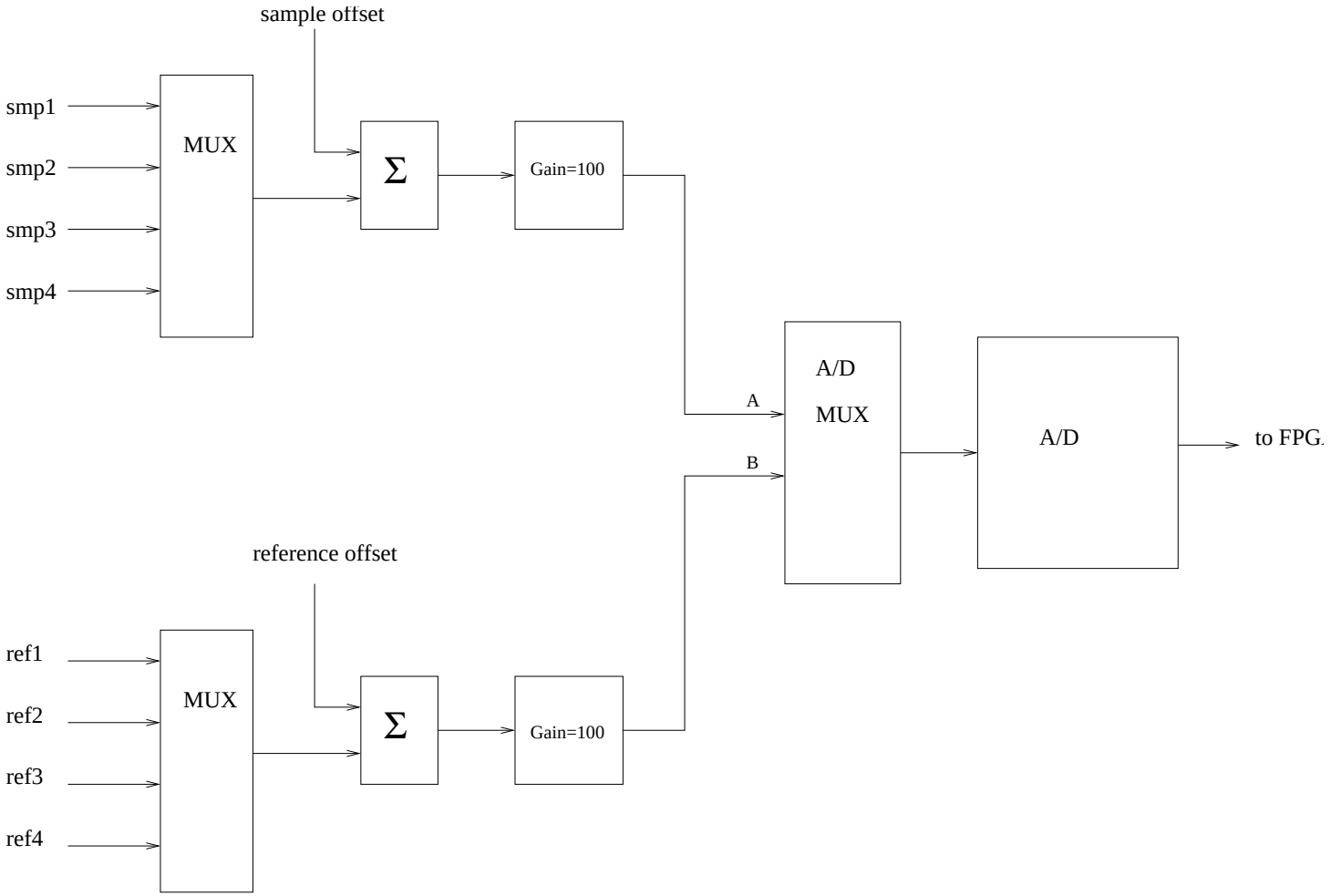

Fig. 2 A/D input connections

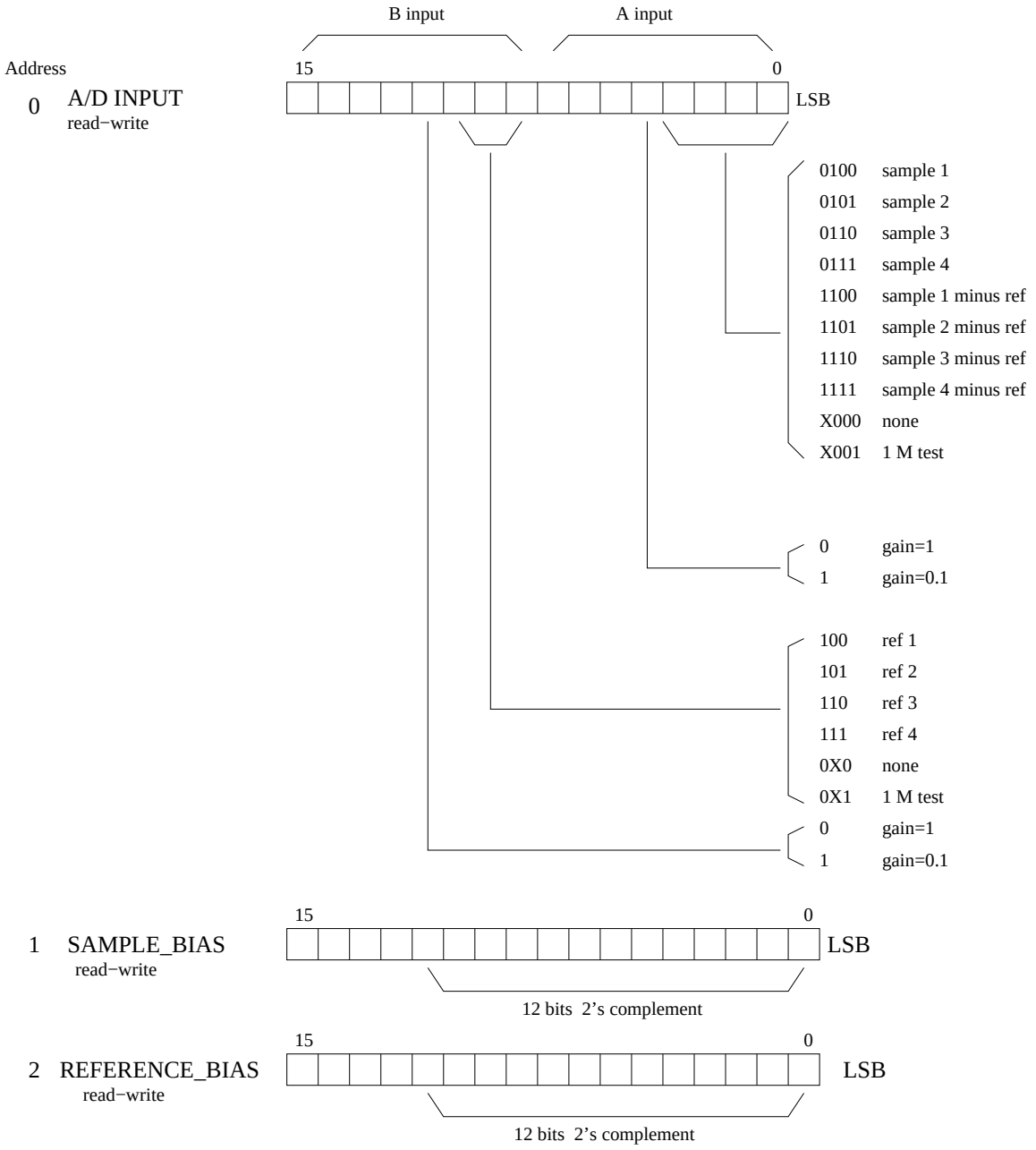

Fig. 3a Register formats

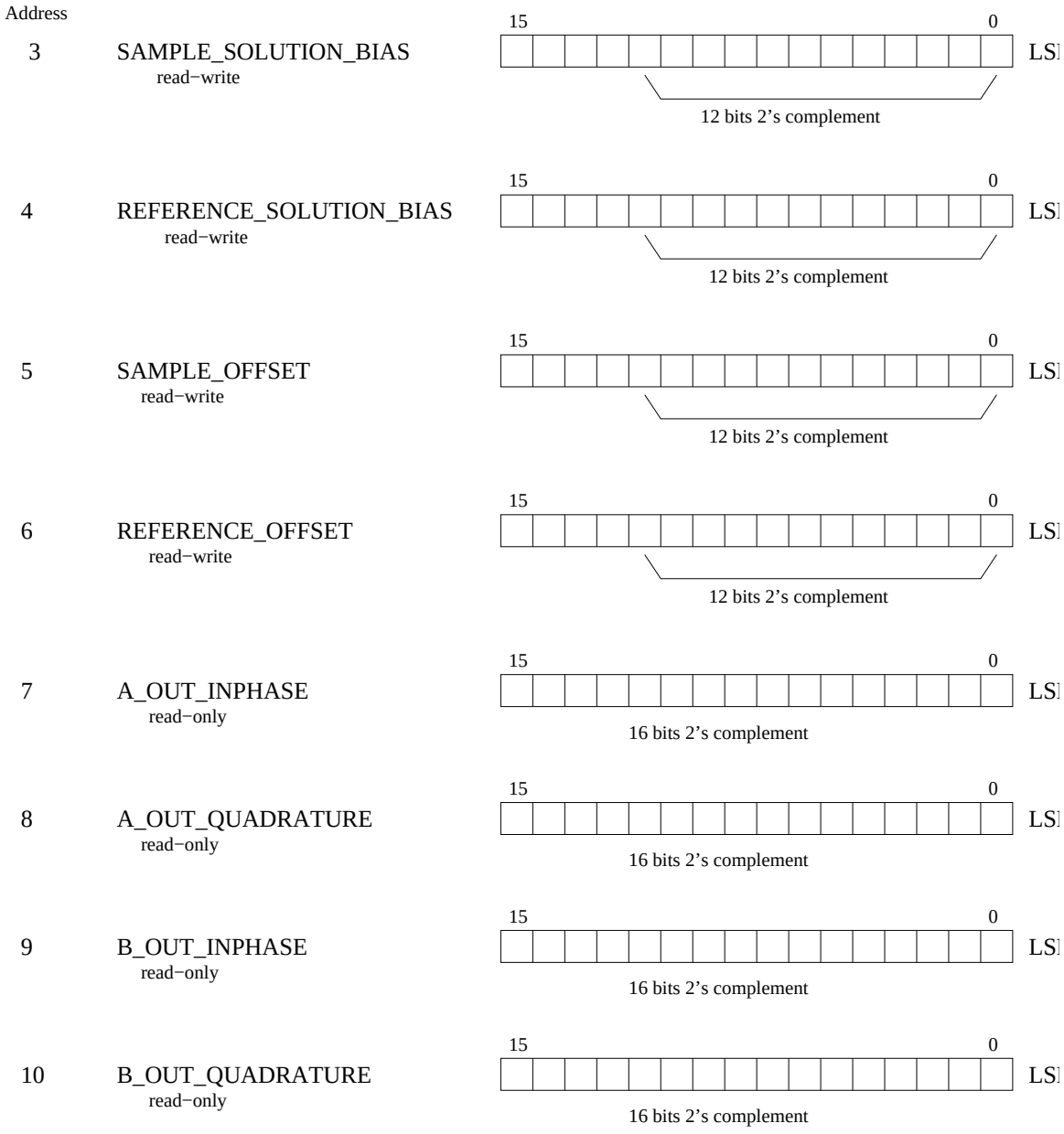

Fig. 3b Register formats

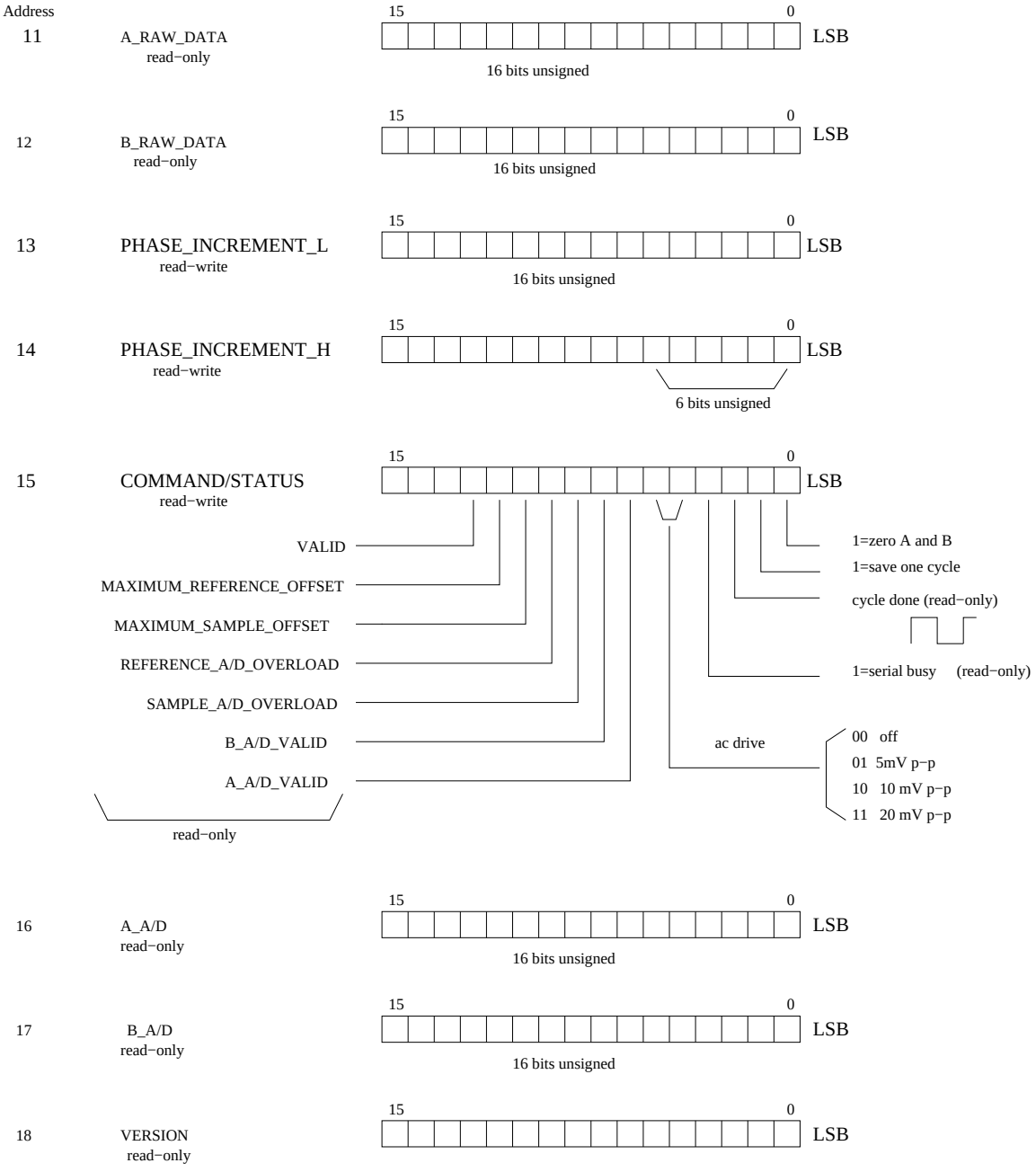

Fig. 3c Register formats