How to Use the Bio-Sensor Electronics

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This document gives a brief description on the use of the bio-sensor electronics to obtain useful information from the sensor FET's. The purpose of the electronics is to determine the dynamic resistance of the sample and reference FET's as a function of the DC drain-to-source voltage applied to the FET's. To perform this task, the electronics provides a variable source of DC drain to source voltage, a low-level sinusoidal drive voltage, and a means for measuring the AC drain-to-source current. The dynamic resistance of the FET at the applied DC drain-to-source voltge is then merely the ratio of the applied AC drive voltage to the measured AC drain current. By repeating this measurement for various drain-to-source voltages, the desired dynamic resistance versus DC drain-to-source voltage function is obtained. Usually these functions would be determined for all eight sensor FET's.

The electronics are controlled by reading and writing some 19 control registers, these being described in the document "Control Registers in the Bio-Sensor FPGA." Some of the registers are intended for test purposes and would probably not need to be accessed in the course of the normal measurement process.

Before describing the process for making measurements, it may be helpful to have some understanding of the internal workings of the electronics.

The voltage supplied to the FET drains consists of a DC value that can range from -2.5V to +2.5V plus a small AC value of 5mV, 10mV or 20mV. Since the AC component is quite small compared to the DC component, the resultant AC drain current (the signal of interest) will also be quite small compared to the DC drain current. Thus, in order to have high resolution of the AC current, it's necessary to cancel (or zero out) most of the DC current before making an AC current measurement. Two offset registers, one for the sample FET's and the other for the reference FET's provide this DC current

cancellation. Note that these offset registers can only cancel DC currents up to 10.24 μamps when the gain is 0.1, or 1.024 μamps using a gain of 1.

After the DC drain currents of the sample and reference FET's have been cancelled, then the AC drain currents are available for readout from the inphase and quadrature registers. Normally only the inphase current would be of interest, but if the quadrature current were a significant fraction of the inphase current, then this would indicate a large amount of reactive current, which in turn might affect how one wished to interpret the current measurement.

A number of status bits serve to indicate the reliability of the AC current measurements, such as whether the A/D converter were overdriven or whether the DC current cancellation was adequate. These bits should always be examined before deciding whether to trust the accuracy of the current measurements.

The AC drive frequency is adjustable over a range of about 1 Hz to 100 Hz, and each inphase and quadrature current measurement is updated at the end of each cycle of the drive frequency. The "cycle_done" status bit should be examined (polled) to determine when new measurements and relevant status bits are available. At a 1 Hz AC drive frequency, one has an entire second to make use of the measurements, but at a 100 Hz drive frequency one would only have 10 mS before the measurements were updated.

1 A typical Measurement Sequence

When a new set of sensor FET's are installed or the solution surrounding the FET's is changed, then one needs to determine the permissible range of the DC drain-to-source voltage for both the sample and reference FET's. Although one might like to select the full range of -2.5V to +2.5V, the 10.24 μamp limitation of the electronics may not allow this.

1. Set the SAMPLE_SOLUTION and/or the REFERENCE_SOLUTION voltages. These are user-determined values. Set the gain to 0.1 for both the sample and reference channels and select a small value for the SAMPLE_BIAS and REFERENCE_BIAS voltages, such as 0.5V.

2. Set the zero bit (the LSB) of the COMMAND_STATUS register to start the internal zeroing operation.

3. When the zero bit is read back as having been cleared, meaning that the zeroing operation has finished, check the MAXIMUM_SAMPLE_OFFSET and MAXIMUM_REFERENCE_OFFSET bits. If either of these is high, then the drain current for the indicated channel (sample or reference) exceeded 10.24 μamps and the bias voltage for that channel needs to be reduced. If one or the other is low, then the corresponding bias voltage may be increased and/or the gain may be changed to 1.

4. Repeat steps 2 through 4 until the maximum gains and bias voltages have been determined. These steps should also be repeated for all four sample and reference FET's. They should also be repeated for negative bias voltages.

After the allowable ranges of bias voltage have been determined, then it is up to the user to decide which sample and reference FET's are to be used to generate the dynamic resistance versus DC bias voltage functions.

Assuming the FET's have been chosen, then the following sequence is used to find the dynamic resistances versus DC bias voltages:

1. Select the AC drive voltage level in the COMMAND_STATUS register and set the initial sample and reference bias voltages.

2. Trigger the zeroing operation and wait for it to finish.

3. Wait for both the cycle_done and VALID bits to be high; then check the SAMPLE_A/D_OVERLOAD and REFERENCE_A/D_OVERLOAD bits. If either is high, then decrease the AC drive level or change the gain, if not already 0.1, to 0.1. If the gain was changed, repeat steps 2 and 3; otherwise just repeat step 3. It's also possible, but not likely, that a MAXIMUM_ OFFSET bit is set. This will require reducing the corresponding bias voltage and then repeating steps 2 and 3.

4. If the cycle_done and VALID bits are both high and neither OVERLOAD bit is high, then the inphase and quadrature data are valid and may be used to determine the dynamic resistances of both the sample and reference FET's.

5. change the bias voltages of both the sample and reference FET's and repeat steps 2 through 5 until all of the intended bias voltages have been tried.

It may not be possible to followe the above sequences exactly. Any time a solution ground voltage, bias voltage, or gain is changed, a zeroing operation must be triggered and completed without a MAXIMUM_ OFFSET bit being set. If a MAXIMUM_ OFFSET bit is set, then the corresponding gain and/or bias must be reduced. The sample and reference channels can be operated separately if so desired; that is, one can just work with the sample channel and ignore the MAXIMUM_OFFSET and A/D_OVERLOAD bits of the reference channel (and vice versa).

2 DC Bias Current Measurement

After a successful zeroing operation, no MAXIMUM_OFFSET bits set, the DC drain current in μamps is equal to the value in the OFFSET register divided by 2000 or 200 for gains of 1 or 0.1 respectively. The static resistance is then the bias voltage divided by this current.

3 The 1 Megohm Test Resistance

The 1 Megohm test resistance is intended to provide a simple test of the electronics; it's not intended to be used for calibration. Selecting this input in the A/D_INPUT register causes the electronics to think that a 1 Megohm resistance has replaced the drain-to-source current path. Due to the way this test resistance is implemented, the dynamic and static resistances should both be negative 1 Megohm values, irrespective of the gain setting.