

Front Panel Data Port Specifications

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Abstract

This standard provides a specification of the protocol and mechanical characteristics of the Front Panel Data Port. This extension to the VME standard consists of a multidrop synchronous parallel non-addressable bus connection between multiple boards in a single chassis. The connection is made to a connector on the front panel of each board by means of an eighty conductor ribbon cable.

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Acknowledgement

The current Front Panel Data Port design is based on earlier work done by Jerome Palmer.

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Comments

(These comments are not part of the FPDP standard. They will be removed after sponsor ballot review.)

Unless directed otherwise, comments on this draft should be addressed to the FPDP Task Group, c/o:

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Thank you in advance for your comments.

1 Introduction

The Front Panel Data Port (FPDP) bus is intended to provide data transfer between two or more VMEbus boards at up to 160MB/s with the lowest possible latency, while not compromising existing VMEbus and other connections on the chassis P1 and P2 connectors. FPDP is connected by means of an 80 conductor ribbon cable connector at the front panel of the VMEbus board. The wiring topology is in the form of a bus. Multiple FPDP busses may coexist in a single VMEbus enclosure.

1.1 Standard Terminology

To avoid confusion and to make very clear the requirements for compliance, many of the paragraphs in this standard are labeled with key words that indicate the type of information that they contain. The key words are listed below:

- Rule
- Recommendation
- Suggestion
- Permission
- Observation

Any text not labeled with one of these key words is a description of the FPDP design or operation and is purely narrative. The key words are used as follows:

Rule chapter.number

Rules form the basic framework of the standard. They are sometimes expressed in text form and sometimes in the form of figures, tables or drawings. All rules must be followed in order to ensure compatibility between designs. Rules are characterized by an imperative style. The upper case words SHALL and SHALL NOT are reserved exclusively for stating rules in this document and are not used for any other purpose.

Recommendation chapter.number

Whenever a recommendation appears, designers would be wise to take the advice given. Doing otherwise might result in some awkward problems or poor performance. Using the recommendations will result in a more robust design achieved in a faster time. The upper case words SHOULD and SHOULD NOT are reserved exclusively for stating recommendations in this document and are not used for any other purpose.

Suggestion chapter.number

A suggestion contains advice which is helpful but not vital. The reader is encouraged to consider the advice before discarding it.

Permission chapter.number

In some cases, a rule does not specifically prohibit a design approach, but the reader may be left wondering whether that approach might not violate the spirit of the rule or whether it might lead to some subtle problem. Permissions provide a clear indication that a certain approach is acceptable and will cause no problems. The upper case word MAY is reserved exclusively for stating permissions in this document and is not used for any other purpose.

Observation chapter.number

Observations do not offer any specific advice. They usually follow naturally from what has just been discussed. They spell out the implications of certain rules and bring attention to things that might otherwise be overlooked. They also give the rationale behind certain rules so that the reader understands why the rule must be followed.

2 Scope and Purpose

2.1 Scope

This document specifies the FPDP digital interface and bus, including the physical and data link layers of the OSI reference model, including the mechanical design.

2.2 Purpose

The purpose of this specification is to allow products to be designed to work with other FPDP products. The degree of interoperability may depend on the layers of functionality above the physical and data link layers. These higher layers are not part of this specification.

2.3 References

- [1] ANSI/IEEE STD1014-1987, VMEbus Specification.
- [2] ISO 7498, Open Systems Interconnection (OSI) Reference Model, Oct., 1984.

3 Definitions

3.1 General

Data Link Layer:	The Open Systems Interconnection (OSI) reference model [2] layer specifying the low level logical protocol.
Physical Layer:	The OSI reference model layer specifying electrical and mechanical specifications.
FPDP Transmitter Master:	A FPDP interface which terminates certain signals and transmits data onto the FPDP bus when the bus is terminated at the receiving end by a FPDP Receiver Master interface, in accordance with this specification.
FPDP Receiver Master:	A FPDP interface which terminates certain signals and receives data from the FPDP bus when the bus is terminated at the transmitting end by a FPDP Transmitter Master interface, in accordance with this specification.
FPDP Receiver:	A FPDP interface which receives data from the FPDP bus when the bus is terminated at one end by an FPDP Transmitter Master and at the other end by a FPDP Receiver Master, in accordance with this specification.
PECL:	Positive Emitter Coupled Logic. An ECL logic family that requires only a +5Volt supply.
Frame:	A frame of data is defined as a sequence of consecutive data for which the start or end of frame is identified by a synchronizing signal. The purpose of this is to allow memory to be correctly initialized before receiving data, and to allow the data for each channel to be correctly identified by the receiving system in cases where a system is processing multi-channel data.
Frame Length:	The number of items of data in a frame.
Unframed Data:	Data which has no particular organization and which, therefore, does not require synchronization to be communicated from the FPDP/TM interface to FPDP/R and FPDP/RM interfaces in order for the data to be used.
Single Frame Data:	Data organized as a single frame, where the start of transmission of the frame is indicated by an assertion of the SYNC* signal prior to the assertion of DVALID*.
Repeating Frame Data:	Data transmitted as a series of frames, where the last item of each frame is marked by the assertion of the SYNC* signal coincidentally with the DVALID* signal. This type of data is further divided into Fixed Size Repeating Frame Data and Dynamic Size Repeating Frame Data.

4 Overview

4.1 General

The FPDP bus is intended to provide high speed transfer of data between two or more VMEbus boards with minimum latency and precisely known transfer rates. The FPDP bus is a 32-bit parallel synchronous bus wired by means of an 80-conductor ribbon cable. A single master device generates a free-running clock (Data Strobe or \pm PECL Data Strobe), the frequency of which defines the maximum transfer rate of the bus. Transfers occur in one direction only; however, interfaces may be capable of being configured by means of hardware links or switches, or under software control, as transmitters or receivers. Since there is only one master, there cannot be contention between devices on the bus. The bus protocol does not include address or arbitration cycles, so the data transfer rate is fully defined by the frequency of Data Strobe. A mechanism is provided to allow a receiver to hold off the transmitter if its memory is almost full; this is done using the Suspend Data signal. A mechanism is also provided to allow synchronization of the receiver to the transmitted data stream to provide for memory initialization and so that channelized (framed) data can be correctly interpreted; this is done using the Sync Pulse signal. An example of a VMEbus chassis containing several boards with multiple FPDP busses is shown in Figure 1.

4.2 VMEbus Compatibility

The FPDP is wired by means of an 80-conductor ribbon cable between single connectors on the front panel of each VMEbus board. The VMEbus P1 and P2 backplane connectors, as well as any other connectors which may be defined by amendments to the VME specification, are therefore unaffected by the use of FPDP.

Permission 4.2.1:

FPDP MAY be used in environments other than VMEbus.

4.3 Interconnectivity

The FPDP is a multi-drop bus intended to carry either framed or unframed data with a single board interface providing timing signals. This interface is referred to as the "FPDP Transmitter Master" (FPDP/TM) in this specification.

Permission 4.3.1:

Multiple FPDP busses MAY exist within a VMEbus chassis, subject to the mechanical constraints of cable and connector positions, and maximum cable length.

Permission 4.3.2:

Each board MAY have more than one FPDP interface, to support separate input or output data paths to or from the board.

Permission 4.3.3:

FPDP busses MAY be used to connect between two separate VMEbus chassis, subject to the maximum cable length specification (see related information in section 7.2).

4.4 Addressing and Multiple Boards

The FPDP bus design does not allow for the transmission of address information, however it is desirable that the bus have the capability to carry data which is multiplexed from multiple boards.

Permission 4.4.1:

Manufacturers MAY design FPDP interfaces such that the FPDP/TM functionality is provided by multiple boards each providing a connection to the FPDP bus.

Observation 4.4.1:

It is not intended that boards from different manufacturers will necessarily be capable of operating together in FPDP/TM groups, since the method of synchronization is not specified in this document. See also Observation 6.1.1.1.

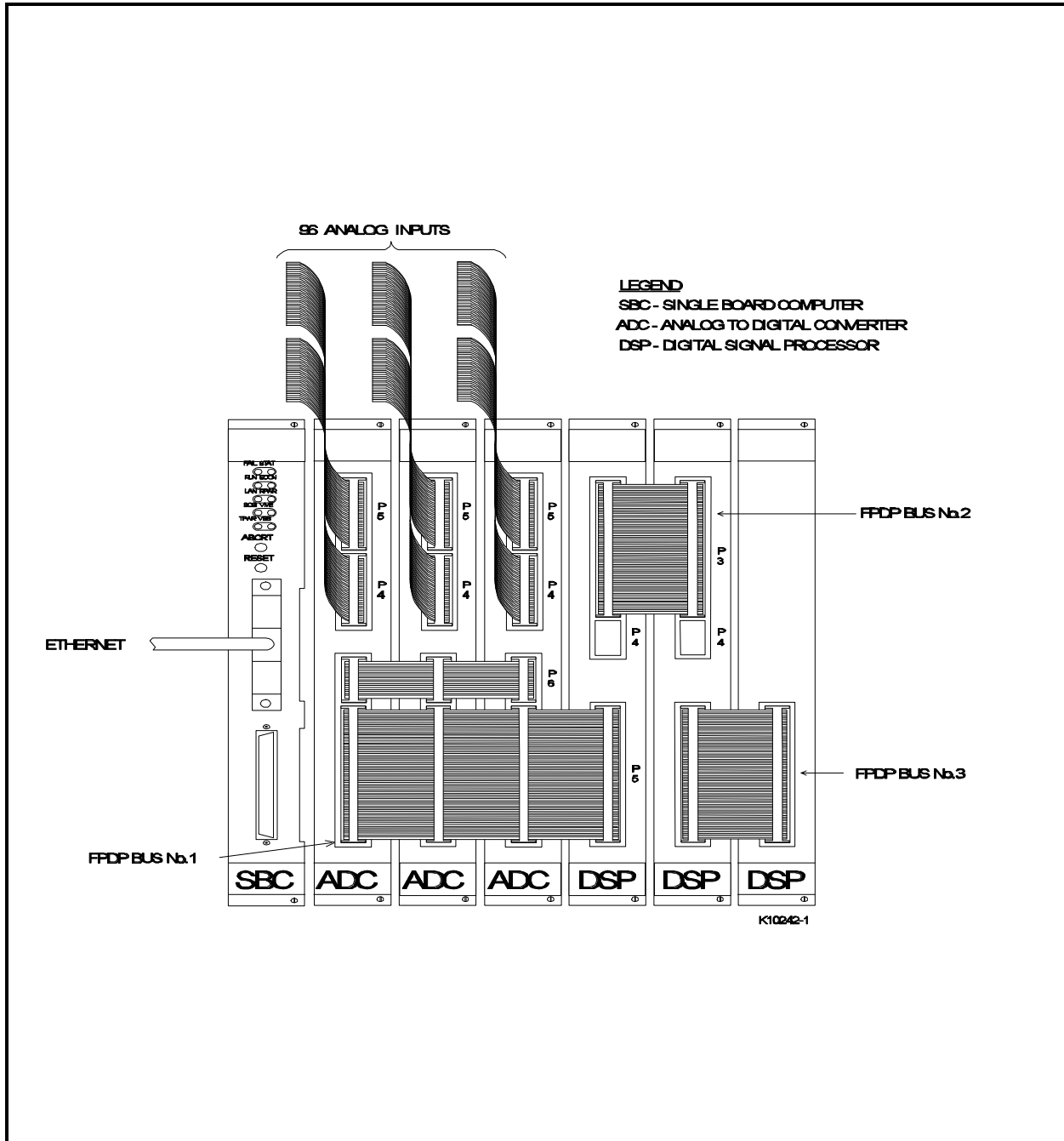


Figure 1 - Example Configuration with Multiple FPDP Buses

5 Data Link Layer Specification

Many applications of FPDP will be with high performance data acquisition and transfer systems. These frequently deal with multiple channels of data. It is essential to have a method for identifying the channel associated with each item of data. The method chosen is to allow for data frames, where each frame is delineated by an assertion of the SYNC* (Sync Pulse) signal. However, this standard also allows for applications where the data is not required to be framed. Several methods of using the SYNC* signal have been identified. The requirements for the SYNC* (Sync Pulse) signal are outlined in section 5.1; this section will review the possible uses for each of the types of synchronization. It is the user's responsibility, should synchronization be required, to determine the type of synchronization needed, and whether a particular interface or interface design supports the required method. The data frame types defined by this standard are as follows:

- Unframed Data
- Single Frame Data
- Fixed Size Repeating Frame Data
- Dynamic Size Repeating Frame Data

Unframed Data interfaces are intended for use where the organization of the data is of no relevance and the FPDP/RM or FPDP/R interface does not need to be informed of a synchronization point in the data stream.

The Single Frame Data and the two Repeating Frame Data type definitions serve the requirements of interfaces which must pass data in response to an event, such as multi-channel A/D converters, line and frame scan devices and devices which transfer fixed length data files. This is accomplished by synchronizing data acquisition at the FPDP/RM or FPDP/R interface to a separate signal, SYNC* (Sync Pulse). In none of these cases is the synchronization signal or event actually included in the data stream; synchronization at the receiving end is accomplished by virtue of holding acquisition off until the SYNC* signal is received.

The three framed data types differ in implementation. In all cases, the synchronization event must occur prior to the data to which it applies, however, in the Single Frame Data interface, the synchronization is intended to occur between blocks, while in both of the Repeating Frame Data types, the synchronization event occurs coincident with the last data word transferred in the block before. As a result, Single Frame Data compliant interfaces require that the synchronization event occurs prior to the data being synchronized, before the assertion of DVALID* (Data Valid). Fixed Size Repeating Frame Data and Dynamic Size Repeating Frame Data compliant interfaces require that the synchronization event occurs at the end of the block prior to that being synchronized, while DVALID* (Data Valid) is still asserted.

As observation 5.1.3 discusses, the very first block of data passed through either of the Repeating Frame Data compliant interfaces will probably not be synchronized, as the first SYNC* (Sync Pulse) assertion will be at the end of that block. System designers should consider this in their plans.

While the intent of the Single Frame Data and both Repeating Frame Data types is similar at the global level, they differ in detail. The concept behind Single Frame Data compliant interfaces is that the synchronization event occurs infrequently, or only once, perhaps. In systems which require synchronization at that frequency, it is likely that the receiver's data path (temporary storage) should also be cleared prior to, or along with, the synchronization event.

The concept behind the Repeating Frame Data types is slightly different, in that the synchronization event should occur frequently: once per scan; or pass through an array: for example, to mark the first channel. In this type of system, the receiver's data path should not require clearing at the same frequency, which would be more difficult due to the requirement that DVALID* (Data Valid) be asserted simultaneously with SYNC* (Sync Pulse).

The difference between Fixed Size Repeating Frame Data and Dynamic Size Repeating Frame Data is that the former permits only frames of the same length, whereas the latter allows frame sizes to vary

from frame to frame in an arbitrary manner, as long as they comply with other requirements of this standard.

Designers of interfaces supporting the framed data types may wish to reject all data received before the first occurrence of SYNC* (Sync Pulse) so that no data is written to the input data path until SYNC* has occurred. In the case of Single Frame data, this would allow the interface to have the data path cleared, and the hardware set up properly for the synchronization event without requiring data to be shut off at the input. In the case of Fixed Size and Dynamic Size Repeating Frame Data, the ability to synchronize each block of data being transferred may add confidence to the system designer's plan.

Timing of the SYNC* (Sync Pulse) signal must meet the same requirements for set-up and hold times as the data signals, indicated elsewhere in the document. Other timing requirements are given in Sections 6.4.1 and 6.4.2.

5.1 Data Frame Format

Four types of data frame format are defined for use on the FPDP bus. These are Unframed Data, Single Frame Data, Fixed Size Repeating Frame Data and Dynamic Size Repeating Frame Data. The frame size is defined as the number of data items in a frame.

Rule 5.1.1:

FPDP Interfaces SHALL be designed to handle either Unframed Data, Single Frame Data, Fixed Size Repeating Frame Data or Dynamic Size Repeating Frame Data, or more than one of these formats.

Rule 5.1.2:

FPDP/RM and FPDP/R interfaces claiming to handle Unframed Data SHALL NOT require the SYNC* (Sync Pulse) signal to be asserted in order to correctly receive data in this mode.

Observation 5.1.1:

When using Unframed Data, the SYNC* (Sync Pulse) signal is not used.

Observation 5.1.2:

When using Single Frame Data, the SYNC* (Sync Pulse) signal is asserted prior to the start of transmission of data, i.e. DVALID* (Data Valid) is not asserted at the same time. SYNC* is not asserted again until the start of the next transmission.

Observation 5.1.3:

When using Fixed Size Repeating Frame Data or Dynamic Size Repeating Frame Data, SYNC* (Sync Pulse) signal is asserted when DVALID* (Data Valid) is asserted, coincident with the last data item of the frame. This means that reception of the first frame may not be synchronized and it should be ignored by the receiving board.

Rule 5.1.3:

When a system uses Single Frame Data or Fixed Size Repeating Frame Data, the frame size SHALL NOT vary from frame to frame.

Observation 5.1.4:

When using Dynamic Size Repeating Frame Data, the frame size may vary from frame to frame in an arbitrary manner.

6 Physical Layer Specification

6.1 Interface Functions

There are three possible functions for a FPDP interface in a FPDP bus configuration. These are "FPDP Transmitter Master" (FPDP/TM), "FPDP Receiver" (FPDP/R) and "FPDP Receiver Master" (FPDP/RM). A minimum FPDP configuration consists of two interfaces joined by a FPDP ribbon cable. One of these interfaces is a FPDP/TM, while the other is a FPDP/RM.

Permission 6.1.1:

Boards MAY contain more than one FPDP interface.

Observation 6.1.1:

For example, one FPDP interface might be an input port, while the other is an output port.

Permission 6.1.2:

FPDP interfaces MAY be reconfigurable by means of links or switches, or under software control to perform either the FPDP/TM or the FPDP/R or the FPDP/RM function.

6.1.1 FPDP/TM Function

The FPDP/TM interface drives data and timing signals onto the FPDP. The FPDP/TM interface also terminates the bus signals at one end of the ribbon cable.

Observation 6.1.1.1:

Permission 4.4.1 states that the FPDP/TM function may be fulfilled using more than one board. For designs where multiple boards can be combined to provide the FPDP/TM function, only one board would terminate FPDP bus signals; it must be located at the end of the bus. It is expected that it would be necessary to provide a separate method for communicating timing information between the boards providing this function; for example, this might be by means of a separate front panel connection.

6.1.2 FPDP/RM Function

The FPDP/RM interface receives data from the FPDP synchronously with the timing signals provided by the FPDP/TM. It also terminates the bus at the opposite end of the cable to the FPDP/TM.

6.1.3 FPDP/R Function

The FPDP/R interface receives data from the FPDP synchronously with the timing signals provided by the FPDP/TM. It does not terminate the bus.

Permission 6.1.3.1:

The FPDP/R function MAY be an alternate function of a FPDP/RM interface selected, for example, by the use of on-board links or switches, or by software control.

Permission 6.1.3.2:

More than one FPDP/R interface MAY be connected to the FPDP bus.

6.2 Signals

A list of the FPDP signals is given in Table 1. Mandatory and recommended behavior of FPDP interfaces is described in later sections.

The two PSTROBE (\pm PECL Data Strobe) signals are Positive Emitter-Coupled Logic signals provided as an optional alternative to the STROB (Data Strobe) signal. It is intended that PSTROBE (\pm PECL Data Strobe) be used when it is necessary to use strobe frequencies greater than 20MHz, when driving FPDP busses connecting more than two boards, or when driving longer cables (see section 7.2). The signals provide the same function as STROB (Data Strobe), but with greater noise immunity.

Recommendation 6.2.1:

Designers SHOULD implement the \pm PSTROBE signals on FPDP/TM, FPDP/R and FPDP/RM interfaces in order to achieve more reliable performance at higher speeds.

Observation 6.2.1:

Users should take care not to allow a loose cable to cause shorting to ground of the PECL signals, when powered, since this may result in the destruction of the driver devices.

6.3 Connectors

Rule 6.3.1:

The FPDP bus interface connector SHALL be either Part Number 8831E-080-170L from KEL Connectors Inc. of Sunnyvale, CA, or Part Number P50E-080P1-RR1-TG from Robinson-Nugent of New Albany, IN, or a compatible connector.

This connector connects 80 conductors in two rows of pins to the mating connector; however, the board pin out is in four rows. Manufacturers' data uses a scheme for numbering the printed circuit board pin out which does not correspond to the cable conductor numbering. Figure 2 shows the board connector with both printed circuit board pin out and cable numbers at the mating face of the connector. The mating connector takes a single ribbon cable of 80 conductors on 25 mil pitch and includes a locking arrangement to prevent unintentional disconnection. The mating connector part number is KEL 8825E-080-175 (with strain relief), KEL 8825R-080-175 (without strain relief) or Robinson-Nugent P25E-080S-TG.

6.3.1 Pinout Correspondence with Cable

The connector pinout on the board consists of four rows of twenty pins. Rows are labelled A through D, while pins are labelled 1 through 20. The connector has an index mark at the bottom right hand side (see Figure 2) when the board is inserted vertically in normal orientation in a VMEbus chassis (but see section 6.3.2 below). The ribbon cable conductors correspond to board pattern pins A1, B1, C1, D1, A2, B2 C2, D2, etc., starting from the index mark.

6.3.2 Connector Orientation

When the FPDP interface connector is located on the main board, the connector index mark will be located at the bottom right hand side of the connector when the board is inserted vertically in a chassis in normal orientation. However, in many designs, the FPDP connector will be located on a mezzanine or daughter board. In this case, it may be necessary to mount the connector on the side of the daughter board closest to the mother board in order to avoid the connector profile exceeding the available chassis slot width. This results in the connector being inverted compared to a connector mounted on a mother board. In this case, the ribbon cable should be wired directly (i.e. without folding) between FPDP connectors irrespective of the connector orientation in the chassis. If a connector is inverted (i.e. index mark at top left hand side), the inverted pinout list given in Table 3 applies. Figure 3 shows an example of a system configuration where some boards are mother board/daughter board combinations with inverted connectors, while others have non-inverted connectors.

Rule 6.3.2.1:

The pinout of signals SHALL be as given in Table 2 when the FPDP connector is in normal orientation, i.e. with the index mark at the bottom right hand side, when the board is vertically mounted.

Recommendation 6.3.2.1:

Designers SHOULD use the inverted connector pin out list given in Table 3 in preference to that given in Table 2 when designing a product with an inverted FPDP connector, in order to avoid the need for folding of the FPDP cable when assembling a system using the product.

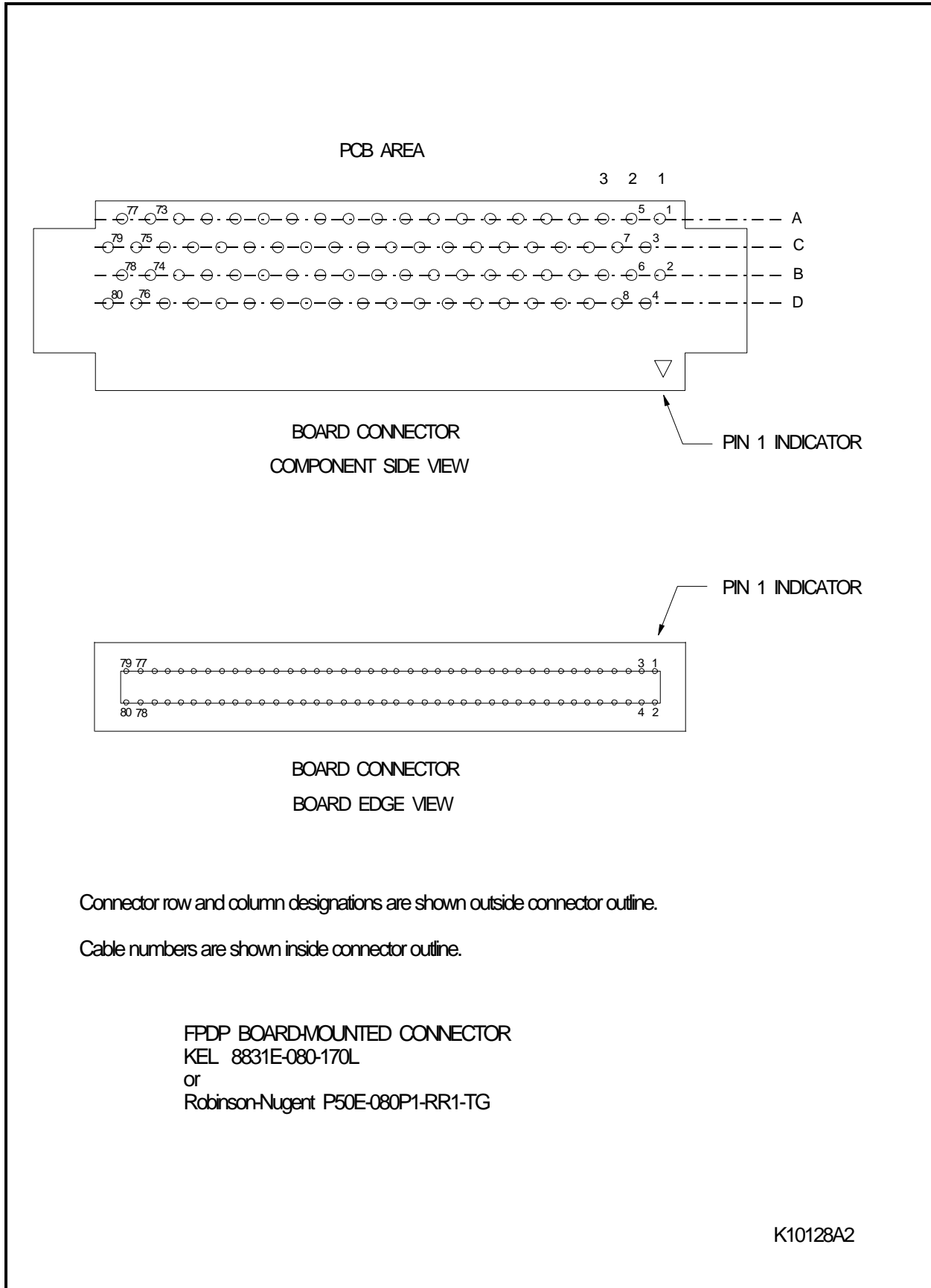


Figure 2 - FPDP Connector Pinout

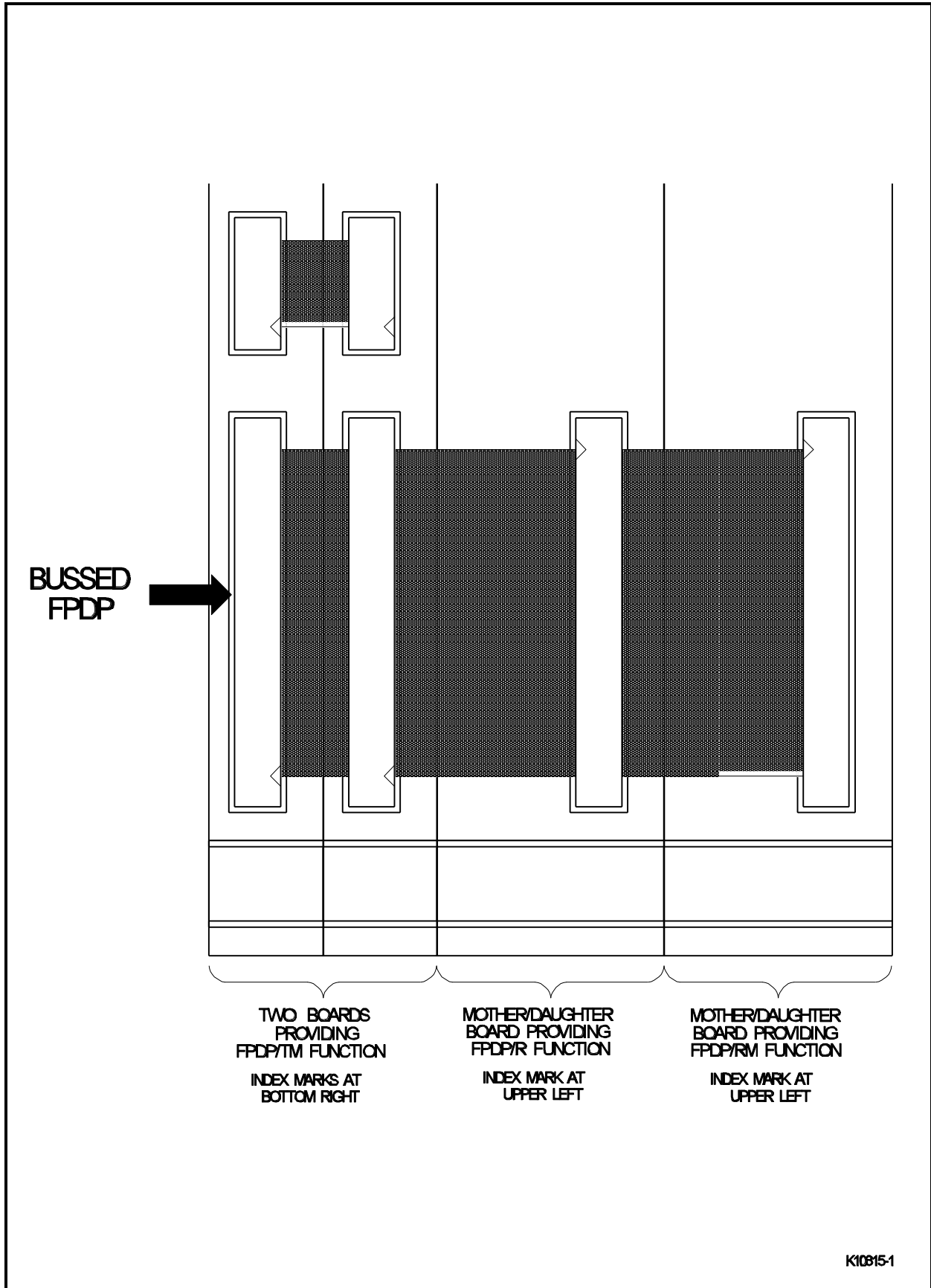


Figure 3 - FPDP Cable with Inverted and Non-Inverted connectors

6.4 Drivers, Receivers and Terminations

Examples of suitable signal driver and receiver device part numbers are given in Table 4. Use of these part numbers is not mandatory, however, care should be taken to ensure that equivalent performance is achieved if substitute parts are used. The requirements for the various interface types to drive and receive each signal are given in the following sections.

Rule 6.4.1:

The terminating resistor values and types for both transmitting and receiving ends given in Table 5 SHALL be used.

Observation 6.4.1:

The values for series terminating resistors have been chosen based on a configuration where a FPDP is bussed across twenty boards, thus providing a worst case configuration from the point of view of drive levels and noise. These values have been used in systems containing a minimum number of boards and have been found to operate satisfactorily.

Rule 6.4.2:

The PSTROBE and PSTROBE* signals, if used, SHALL be terminated using Method 1 as specified in Table 5.

Observation 6.4.2:

Method 1 PSTROBE / PSTROBE* termination has been more commonly used in products predating this standard. However, Method 2 termination is preferable since it is symmetrical i.e. it allows interfaces to be reconfigured between FPDP/TM and FPDP/RM or FPDP/R functions without changing the termination network.

Recommendation 6.4.1:

If possible, Method 2 termination SHOULD be provided in addition to Method 1, if PSTROBE / PSTROBE* signals are supported. The two termination methods could be switchable by wire links, for example.

Rule 6.4.3:

For all signals except the data lines, D<31:00>, terminating resistors SHALL be connected to the signals on interfaces providing the FPDP/TM or FPDP/RM functions, and not on FPDP/R interfaces.

Observation 6.4.3:

The termination resistors are intended to be connected on boards located at each end of the FPDP cable only. No other boards connected to the cable should have the resistors connected, with the exception of the series resistors used on the D<31:00> (Data Bus) lines which are intended to be in circuit on all FPDP/TM boards.

Permission 6.4.1:

Where it is required to provide a bidirectional interface, the series terminating resistors specified for the data lines, D<31:00>, on the FPDP/TM function MAY be retained in circuit while the interface is operating as the FPDP/RM or the FPDP/R functions.

Observation 6.4.4:

Thus the terminating resistors would be in circuit at both ends of the transmission line. This situation is acceptable.

6.4.1 FPDP/TM Interfaces

Rule 6.4.1.1:

FPDP/TM interfaces SHALL drive the following signals:

D<31:00>	(Data Bus)
DIR*	(Data Direction)
DVALID*	(Data Valid)
STROBE	(Data Strobe)

Rule 6.4.1.2:

Designers SHALL observe the timing parameters given in Table 6 when using the TTL STROB (Data Strobe) signal, or Table 7 when using the PECL PSTROBE, PSTROBE* (\pm PECL Strobe) signals, with reference to Figures 4 and 5.

Rule 6.4.1.3:

DVALID* (Data Valid) SHALL NOT be asserted until at least 16 full cycles of STROB (Data Strobe) and PSTROBE, PSTROBE* (\pm PECL Strobe) have occurred.

Rule 6.4.1.4:

The STROB (Data Strobe) and PSTROBE, PSTROBE* (\pm PECL Strobe) signals SHALL run continuously, once data transfer has been started on the bus, until data transfer is complete.

Observation 6.4.1.1:

The timing parameters given in Table 6 relate to a maximum frequency of 20MHz for the STROB (Data Strobe) TTL signal, while those given in Table 7 relate to a maximum frequency of 40MHz for the PSTROBE, PSTROBE* (\pm PECL Strobe) signal. However, operation at higher frequencies may be possible, depending on the implementation.

Rule 6.4.1.5:

Unused D<31:00> (Data Bus) lines SHALL be connected to ground through a high value resistor.

Suggestion 6.4.1.1:

A resistor value of 10kOhm is suitable to connect an unused data line to ground.

Observation 6.4.1.2:

Which of the thirty-two D<31:00> (Data Bus) signals are driven, and which are not driven by FPDP/TM interfaces is optional and will depend on various factors. For example, a fourteen bit Analog-to-Digital converter board would probably not drive all lines, but might drive only 14 signals. Alternatively it might drive 28 signals, corresponding to two data per strobe period.

Rule 6.4.1.6:

FPDP/TM interfaces SHALL NOT drive data onto the FPDP until the NRDY* (Not Ready) signal is negated by FPDP/RM and FPDP/R interfaces.

Rule 6.4.1.7:

FPDP/TM interfaces SHALL drive DIR* (Data Direction), to the asserted (low) state during at least 16 cycles of the STROBE (Data Strobe) and PSTROBE, PSTROBE* (\pm PECL Data Strobe) signals before the assertion of DVALID* (Data Valid).

Permission 6.4.1.1:

Assertion and negation of the DIR* (Data Direction) signal MAY be asynchronous with other FPDP signals.

Rule 6.4.1.8:

FPDP/TM interfaces SHALL drive their data onto the FPDP D<31:00> (Data Bus) lines synchronously with STROBE (Data Strobe) and PSTROBE, PSTROBE* (\pm PECL Data Strobe) and while asserting DVALID* (Data Valid), in accordance with the timing diagram of Figure 4.

Rule 6.4.1.9:

If the PSTROBE, PSTROBE* (\pm PECL Data Strobe) signals are implemented, they and STROBE (Data Strobe) SHALL operate synchronously.

Rule 6.4.1.10:

When operating in Single Frame Data mode, FPDP/TM interfaces SHALL assert SYNC* (Sync Pulse) prior to the first element of data being transmitted, in accordance with the timing diagram of Figure 5(a).

Rule 6.4.1.11:

When operating in Fixed Size or Dynamic Size Repeating Frame Data mode, FPDP/TM interfaces SHALL assert SYNC* (Sync Pulse) coincidentally with the last element of data in every frame, in accordance with the timing diagram of Figure 5(b).

Observation 6.4.1.3:

When generating Fixed Size or Dynamic Size Repeating Frame Data with a frame size of one, the SYNC* (Sync Pulse) signal will be continuously asserted.

Rule 6.4.1.12:

When operating in Fixed Size or Dynamic Size Repeating Frame Data mode, FPDP/TM interfaces SHALL assert DVALID* (Data Valid) simultaneously with SYNC* (Sync Pulse) in accordance with the timing diagrams of Figures 4 and 5(b).

Rule 6.4.1.13:

FPDP/TM interfaces SHALL receive the following signals:

NRDY*	(Not Ready)
SUSPEND*	(Suspend Data)

Rule 6.4.1.14:

FPDP/TM interfaces SHALL negate the DVALID* (Data Valid) signal and suspend transmission of data within 16 cycles of STROBE (Data Strobe) or PSTROBE, PSTROBE* (\pm PECL Data Strobe) following assertion of the SUSPEND* (Suspend Data) signal by the FPDP/R or FPDP/RM interface.

Recommendation 6.4.1.1:

FPDP/TM interfaces SHOULD observe a delay following assertion of the SUSPEND* (Suspend Data) signal to prevent possible instability problems, since SUSPEND* need not be synchronous with other signals. One possible method of doing this is to sample the SUSPEND* signal using the rising edge of STROB (Data Strobe) or PSTROBE, PSTROBE* (\pm PECL Data Strobe), if supported, on two successive cycles before processing it.

Rule 6.4.1.15:

Following negation of DVALID* (Data Valid), FPDP/TM interfaces SHALL NOT assert the DVALID* signal until the SUSPEND* (Suspend Data) signal has been negated.

Observation 6.4.1.4:

The objective of the Suspend Data mechanism is to avoid loss of data.

Permission 6.4.1.2:

Designers of FPDP interfaces MAY implement transmitters and/or receivers for either or both of the PIO1, PIO2 (Programmable I/O) signals on FPDP/TM interfaces.

Rule 6.4.1.16:

The FPDP cable pins allocated to the PIO1, PIO2 (Programmable I/O) signals are reserved, and SHALL NOT be used for any other purpose (see Tables 2 and 3 for pin allocations).

Observation 6.4.1.5:

The PIO1 and PIO2 signals are ancillary signals and are not required for the core FPDP function. They provide a means for FPDP/TM and FPDP/R- interfaces to communicate information which is not specified in this standard. If the drivers and/or receivers are implemented on an interface, the purpose for which they are used is user-defined.

Rule 6.4.1.17:

If a FPDP/TM interface has transmit capability on one or both PIO1, PIO2 (Programmable I/O) signal lines, it SHALL NOT drive these lines following application of power to the interface.

Observation 6.4.1.6:

This is to avoid the possibility of two interfaces in a system driving the lines at the same time and causing destruction of driver devices.

6.4.2 FPDP/RM and FPDP/R Interfaces

In this section, the terminology FPDP/R- is used to indicate that a Rule, Recommendation, Suggestion, Permission or Observation applies to both FPDP/RM and FPDP/R interfaces.

Permission 6.4.2.1:

FPDP/R- interfaces MAY assert the following signals:

NRDY*	(Not Ready)
SUSPEND*	(Suspend Data)

Rule 6.4.2.1:

Designers SHALL observe the timing parameters given in Table 6 when using the TTL STROB (Data Strobe) signal, or Table 7 when using the PECL PSTROBE, PSTROBE* (\pm PECL Strobe) signals, with reference to Figures 4 and 5.

Rule 6.4.2.2:

FPDP/R- interfaces SHALL negate the NRDY* (Not Ready) signal when they are ready to accept data.

Permission 6.4.2.2:

Assertion and negation of the NRDY* (Not Ready) signal MAY be asynchronous with other FPDP signals.

Rule 6.4.2.3:

FPDP/R- interfaces SHALL assert the SUSPEND* (Suspend Data) signal when they are approaching a state of being unable to accept more data, but can accept data for at least sixteen more cycles of STROBE (Data Strobe).

Observation 6.4.2.1:

The objective of the Suspend Data mechanism is to avoid loss of data. If a particular receiver interface can never be in danger of losing data, it may not be necessary to implement this capability.

Permission 6.4.2.3:

Assertion and negation of the SUSPEND* (Suspend Data) signal MAY be asynchronous with other FPDP signals.

Rule 6.4.2.4:

FPDP/R- interfaces SHALL receive the following signals:

D<31:00>	(Data Bus)
DVALID*	(Data Valid)
STROBE	(Data Strobe)

Recommendation 6.4.2.1:

FPDP/R- interfaces SHOULD have the capability to receive and use all thirty-two D<31:00> (Data Bus) signals.

Rule 6.4.2.5:

FPDP/R- interfaces SHALL sample the D<31:00> (Data Bus) and DVALID* (Data Valid) signals using the rising edge of STROBE (Data Strobe) or PSTROBE, PSTROBE* (\pm PECL Data Strobe), if supported, as the clock signal.

Rule 6.4.2.6:

FPDP/R- interfaces SHALL consider data valid only when DVALID* (Data Valid) is asserted.

Rule 6.4.2.7:

FPDP/R- interfaces SHALL have the capability to receive the SYNC* (Sync Pulse) signal if Single Frame or Fixed Size or Dynamic Size Repeating Frame Data are supported.

Rule 6.4.2.8:

When using the SYNC* (Sync Pulse) signal, FPDP/R- interfaces SHALL sample SYNC* on the rising edge of STROB (Data Strobe) or PSTROBE, PSTROBE* (\pm PECL Data Strobe), if supported.

Rule 6.4.2.9:

When operating in Single Frame Data mode, FPDP/R- interfaces SHALL use the SYNC* (Sync Pulse) signal, when asserted, as an indication that data received on the next cycle of STROB (Data Strobe) or PSTROBE, PSTROBE* (\pm PECL Data Strobe) which is qualified by assertion of DVALID* (Data Valid) is the first data of the frame, in accordance with the timing diagram of Figure 5(a).

Rule 6.4.2.10:

When operating in Fixed Size or Dynamic Size Repeating Frame Data modes, FPDP/R- interfaces SHALL use the SYNC* (Sync Pulse) signal, when asserted coincidentally with the DVALID* (Data Valid) signal, as an indication that the current data is the last element of data in the current frame, in accordance with the timing diagram of Figure 5(b).

Permission 6.4.2.4:

Designers of FPDP interfaces MAY implement transmitters and/or receivers for either or both of the PIO1, PIO2 (Programmable I/O) signals on FPDP/R- interfaces.

Rule 6.4.2.11:

The FPDP cable pins allocated to the PIO1, PIO2 (Programmable I/O) signals are reserved, and SHALL NOT be used for any other purpose (see Tables 2 and 3 for pin allocations).

Observation 6.4.2.2:

The PIO1 and PIO2 signals are ancillary signals and are not required for the core FPDP function. They provide a means for FPDP/TM and FPDP/R- interfaces to communicate information which is not specified in this standard. If the drivers and/or receivers are implemented on an interface, the purpose for which they are used is user-defined.

Rule 6.4.2.12:

If a FPDP/R- interface has transmit capability on one or both PIO1, PIO2 (Programmable I/O) signal lines, it SHALL NOT drive these lines following application of power to the interface.

Observation 6.4.2.3:

This is to avoid the possibility of two interfaces in a system driving the lines at the same time and causing destruction of driver devices.

Permission 6.4.2.5:

FPDP/R- interfaces MAY receive the DIR* (Data Direction) signal. Possible uses of this signal are to provide a status indication available to be read by software, or to allow operation to be inhibited until DIR* (Data Direction) is driven to the low state by a FPDP/TM interface.

6.5 Chassis Slot Positions

Observation 6.5.1:

Requirements mandated in other sections of this standard specify that terminating resistors and bus drivers and receivers shall be connected on FPDP/TM and FPDP/RM interfaces only, with the exception of D<31:00> (Data Bus) signal lines. In order to ensure correct termination of bus signals, it is intended that the FPDP/TM interface should be inserted at one end of each FPDP bus, while the FPDP/RM should be inserted at the opposite end. FPDP/R interfaces should be inserted between FPDP/TM and FPDP/RM interfaces.

6.6 Timing

Observation 6.6.1:

It is mandated elsewhere in this standard that FPDP interfaces shall conform to the specifications for STROBE (Data Strobe) and PSTROBE, PSTROBE* (\pm PECL Data Strobe) timing, setup and hold times given in Table 6 and Table 7, and to the timing diagrams for the FPDP bus given in Figures 4 and 5.

6.7 Design Rules

Designers should be careful to observe good design practice when positioning components and laying out signal traces on circuit boards. Components driving and receiving FPDP signals should be placed as close as possible to the FPDP connector.

Recommendation 6.7.1:

Stub lengths for TTL signals SHOULD NOT exceed 50 mm (2 inches) in length.

Recommendation 6.7.2:

Stub lengths for PECL signals SHOULD NOT exceed 25 mm (1 inch) in length.

6.8 Cabling

Observation 6.8.1:

The FPDP bus is designed to use standard 80 conductor ribbon cable of 25 mil pitch. Users should be aware of differences in the characteristics of different types of ribbon cable.

Recommendation 6.8.1:

Users SHOULD employ ribbon cable having a characteristic impedance greater than 75 Ohms when measured between the signal conductor and ground using the industry standard GSG (Ground-Signal-Ground) method, in which conductors adjacent to the measured conductor are grounded at each end.

7 Mechanical Specification

7.1 Connector Vertical Positioning

Recommendation 7.1.1:

FPDP connectors SHOULD be located on VMEbus boards in one or more of the positions shown in Figure 6.

7.2 Cable Length

Rule 7.2.1:

FPDP interfaces SHALL operate with a cable length of up to 1 metre when used in multi-drop configurations.

Rule 7.2.2:

FPDP interfaces SHALL operate with a cable length of up to 2 metres when using STROB (Data Strobe), when used in point-to-point configurations, i.e. when only two interfaces are connected.

Rule 7.2.3:

FPDP interfaces SHALL operate with a cable length of up to 5 metres when using PSTROBE, PSTROBE* (\pm PECL Data Strobe), when used in point-to-point configurations, i.e. when only two interfaces are connected.

Observation 7.2.1:

The maximum cable length which can successfully be used will depend on factors such as the number of boards connected to the FPDP cable and whether the cable is used to connect boards located in different chassis. Using the PSTROBE, PSTROBE* (\pm PECL Data Strobe) signals rather than STROBE (Data Strobe) will tend to increase the maximum usable cable length.

Table 1 - FPDP Signals

SIGNAL	NAME	COMMENTS
D<31:00>	Data Bus	32-bit data bus driven by FPDP/TM Interfaces.
DIR*	Data Direction	The FPDP/TM asserts DIR* low.
DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the FPDP/TM.
STROB	Data Strobe	STROB is a free running clock supplied by the FPDP/TM. FPDP/R and FPDP/RM interfaces should sample the data with the rising edge of STROB when DVALID* is asserted.
NRDY*	Not Ready	NRDY* should be asserted by FPDP/R or FPDP/RM interfaces, when they are not ready to receive data. The FPDP/TM should sample this signal until the FPDP/R or FPDP/RM brings it high, at which time the transfer should commence. Since NRDY* is asynchronous to STROB, the FPDP/TM should double-synchronize to it before sampling its state; this avoids metastability problems.
PIO1, PIO2	Programmable I/O	The PIO signals are programmable I/O lines. They may be configured as inputs or outputs.
PSTROBE	+PECL Data Strobe	This signal along with PSTROBE* may be generated by the FPDP/TM as an optional differential \pm PECL data strobe. PSTROBE is the positive version of the differential clock and has the same polarity as STROB. For high data rate applications, the differential \pm PECL data strobe should be used instead of STROB.
PSTROBE*	-PECL Data Strobe	This signal is the negative version of the differential PECL data strobe.
Reserved		No connection should be made to reserved signals.
SUSPEND*	Suspend Data	SUSPEND* should be generated by FPDP/R or FPDP/RM interfaces to inform the data source of a pending buffer overflow condition. The FPDP/TM may delay for no more than 16 cycles in total before suspending the transfer by negating DVALID*. Since SUSPEND* is asynchronous to STROB, the FPDP/TM should double-synchronize to it before sampling its state; this avoids metastability problems.
SYNC*	Sync Pulse	The FPDP/TM must provide a Sync pulse to FPDP/R and FPDP/RM interfaces to synchronize data transfers when transmitting Single Frame data, Fixed Size Repeating Frame data or Dynamic Size Repeating Frame data. FPDP/R and FPDP/RM interfaces should wait for the Sync pulse before accepting data. FPDP/R and FPDP/RM interfaces should start to accept data on the first Data Valid period following the Sync pulse.

Table 2 - FPDP Non-Inverted Connector Pin Assignments

Cable conductor numbers are shown in brackets. Pin 1 is adjacent to connector index mark.

PIN	ROW A	ROW B	ROW C	ROW D
1	GND (1)	STROB (2)	GND (3)	GND (4)
2	GND (5)	GND (6)	NRDY* (7)	GND (8)
3	DIR* (9)	GND (10)	RESERVED (11)	GND (12)
4	SUSPEND* (13)	GND (14)	GND (15)	GND (16)
5	PIO2 (17)	GND (18)	PIO1 (19)	GND (20)
6	RESERVED (21)	GND (22)	RESERVED (23)	GND (24)
7	PSTROBE (25)	GND (26)	PSTROBE* (27)	GND (28)
8	SYNC* (29)	GND (30)	DVALID* (31)	GND (32)
9	D31 (33)	D30 (34)	GND (35)	D29 (36)
10	D28 (37)	GND (38)	D27 (39)	D26 (40)
11	GND (41)	D25 (42)	D24 (43)	GND (44)
12	D23 (45)	D22 (46)	GND (47)	D21 (48)
13	D20 (49)	GND (50)	D19 (51)	D18 (52)
14	GND (53)	D17 (54)	D16 (55)	GND (56)
15	D15 (57)	D14 (58)	GND (59)	D13 (60)
16	D12 (61)	GND (62)	D11 (63)	D10 (64)
17	GND (65)	D09 (66)	D08 (67)	GND (68)
18	D07 (69)	D06 (70)	GND (71)	D05 (72)
19	D04 (73)	GND (74)	D03 (75)	D02 (76)
20	GND (77)	D01 (78)	D00 (79)	GND (80)

Table 3 - FPDP Inverted Connector Pin Assignments

Cable conductor numbers are shown in brackets. Pin 80 is adjacent to connector index mark.

PIN	ROW A	ROW B	ROW C	ROW D
1	GND (80)	D00 (79)	D01 (78)	GND (77)
2	D02 (76)	D03 (75)	GND (74)	D04 (73)
3	D05 (72)	GND (71)	D06 (70)	D07 (69)
4	GND (68)	D08 (67)	D09 (66)	GND (65)
5	D10 (64)	D11 (63)	GND (62)	D12 (61)
6	D13 (60)	GND (59)	D14 (58)	D15 (57)
7	GND (56)	D16 (55)	D17 (54)	GND (53)
8	D18 (52)	D19 (51)	GND (50)	D20 (49)
9	D21 (48)	GND (47)	D22 (46)	D23 (45)
10	GND (44)	D24 (43)	D25 (42)	GND (41)
11	D26 (40)	D27 (39)	GND (38)	D28 (37)
12	D29 (36)	GND (35)	D30 (34)	D31 (33)
13	GND (32)	DVALID* (31)	GND (30)	SYNC* (29)
14	GND (28)	PSTROBE* (27)	GND (26)	PSTROBE (25)
15	GND (24)	RESERVED (23)	GND (22)	RESERVED (21)
16	GND (20)	PIO1 (19)	GND (18)	PIO2 (17)
17	GND (16)	GND (15)	GND (14)	SUSPEND* (13)
18	GND (12)	RESERVED (11)	GND (10)	DIR* (9)
19	GND (8)	NRDY* (9)	GND (6)	GND (5)
20	GND (4)	GND (3)	STROB (2)	GND (1)

Table 4 - Examples of FPDP Drivers and Receivers

SIGNAL	TRANSMITTER	RECEIVER
D<31:00>	IDT 74FCT16952	IDT 74FCT16952
STROB	IDT 49FCT806A	IDT 49FCT806A
DVALID*, SYNC*	IDT 74FCT16245	IDT 74FCT16952
PSTROBE, PSTROBE*	Motorola MC10ELT28D	Motorola MC10ELT28D
PIO1, PIO2	IDT 74FCT16245	IDT 74FCT16245
SUSPEND*, DIR*, NRDY*	Signetics 74F3038 Open collector	

Note: The terminology “transmitter” and “receiver” in this table refers to the device driving or receiving the signal, respectively, rather than the interface function, FPDP/TM, FPDP/RM or FPDP/R. Thus, a device transmitting D<31:00> will be located on an FPDP/TM interface, while a device transmitting SUSPEND* will be located on an FPDP/RM or FPDP/R interface.

Table 5 - FPDP Terminations

SIGNAL	DRIVER TERMINATION	RECEIVER TERMINATION
D<31:00>	27 Ohm series	
STROB		220 Ohm / 330 Ohm Pull-up / Pull-down
DVALID*, SYNC*	27 Ohm series	
PSTROBE, PSTROBE* (Method 1)	330 Ohm to ground on both + and - wires	110 Ohm across + and - wires
PSTROBE, PSTROBE* (Method 2)	167 Ohm / 250 Ohm Pull up / Pull down on each wire	167 Ohm / 250 Ohm Pull up / Pull down on each wire
PIO1, PIO2	27 Ohm series	
SUSPEND*, DIR*, NRDY*		220 Ohm / 330 Ohm Pull-up / Pull-down
All resistors shall be 5% tolerance or better		

Note: The terminology “transmitter” and “receiver” in this table refers to the device driving or receiving the signal, respectively, rather than the interface function, FPDP/TM, FPDP/RM or FPDP/R. Thus, a device transmitting D<31:00> will be located on an FPDP/TM interface, while a device transmitting SUSPEND* will be located on an FPDP/RM or FPDP/R interface.

Table 6 - FPDP Timing Specifications when using TTL STROBE (Data Strobe)

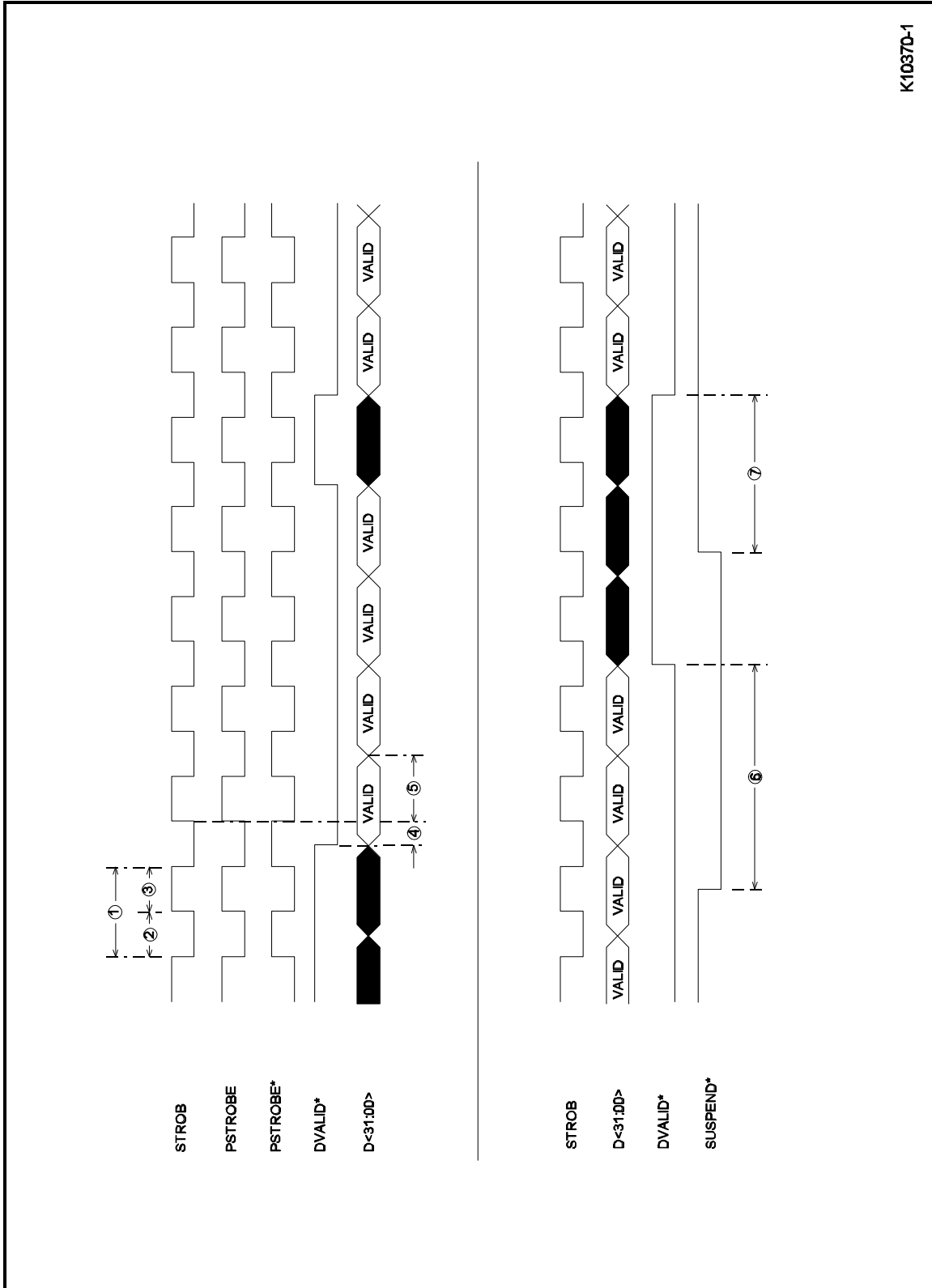
	PARAMETER	At Transmitter End of Cable	At Receiver End of Cable
1	STROB period	50 ns min.	50 ns min.
2	STROB low	22 ns min.	22 ns min.
3	STROB high	22 ns min.	22 ns min.
4	DATA, DVALID* & SYNC* Setup to STROB rising edge	6.0 ns min.	5.0 ns min.
5	DATA, DVALID* & SYNC* Hold from STROB rising edge	12.8 ns min.	11.8 ns min.
6	SUSPEND* to DVALID* negated	16 STROB max.	16 STROB max.
7	SUSPEND* negated to DVALID* re-asserted	1 STROB min.	1 STROB min.

Note: Parameters 4 and 5 refer to both rising and falling edge transitions of DATA, DVALID* AND SYNC*.

Table 7 - FPDP Timing Specifications for PECL PSTROBE (+/- PECL Data Strobe)

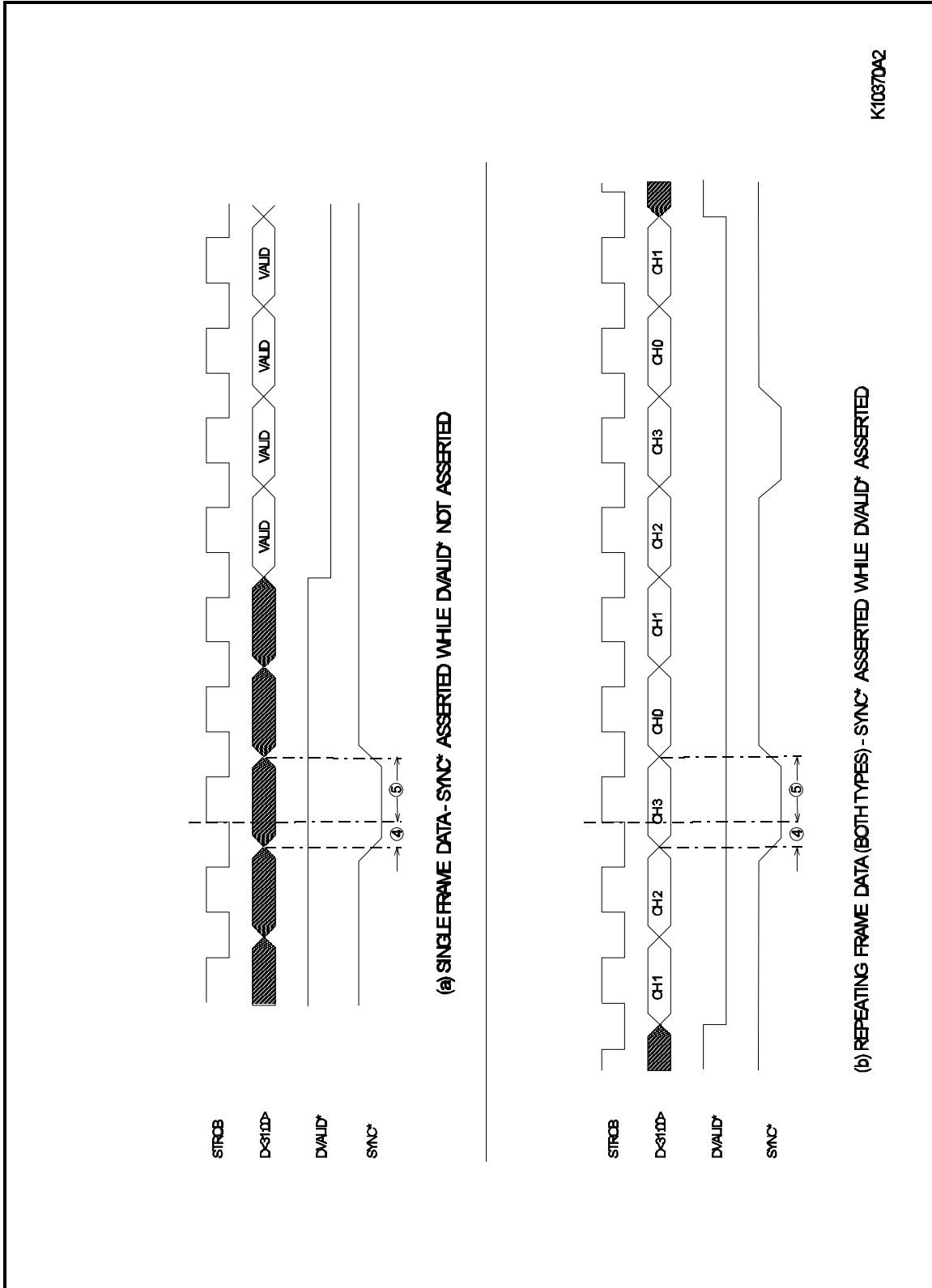
	PARAMETER	At Transmitter End of Cable	At Receiver End of Cable
1	STROB period	25 ns min.	25 ns min.
2	STROB low	10 ns min.	10 ns min.
3	STROB high	10 ns min.	10 ns min.
4	DATA, DVALID* & SYNC* Setup to STROB	5.5 ns min.	4.5 ns min.
5	DATA, DVALID* & SYNC* Hold from STROB	12.0 ns min.	11.0 ns min.
6	SUSPEND* to DVALID* negated	16 STROB max.	16 STROB max.
7	SUSPEND* negated to DVALID* re-asserted	1 STROB min.	1 STROB min.

Note: Parameters 4 and 5 refer to both rising and falling edge transitions of DATA, DVALID* AND SYNC*.



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Figure 4 - FPDP Timing Diagrams - All Data Framing Types



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Figure 5 - FPDP Timing Diagrams - Single Frame Data and Both Repeating Frame Data Types

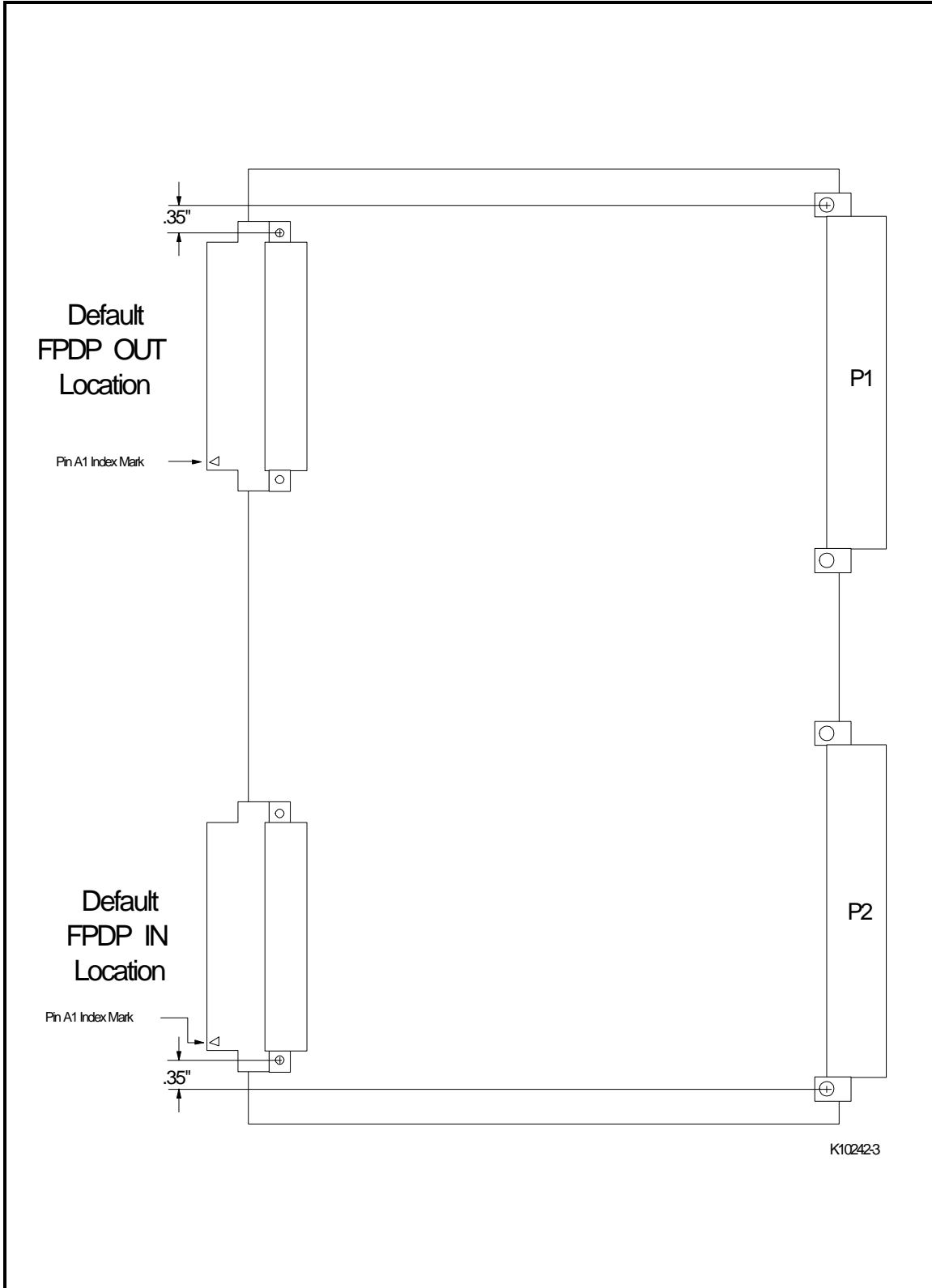


Figure 6 - FPDP Connector Positioning