

PC-MIP Link Receiver Board Implementation Report

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Based on

“PC-MIP Link Receiver Board Specification”

E. Hazen, E. Machado Boston University. Rev 0.9, December 20, 1999

http://ohm.bu.edu/~hazen/my_d0/TxRx/Rx_spec_eh.pdf

Current LRB firmware revision number: 19.

1 Internal structure.

Design consists of the following internal blocks:

- Hamming[2..0] - Hamming code error detection/correction
- LVDS[2..0] - LVDS and PCI FIFO interaction
- RAM - ZBT SSRAM interface
- PCI - PCI interface
- LRBv2 - Main module
- MUX_VHD – optimized PCI data readout multiplexer. Written on VHDL. Synthesized with Synplicity Synplify v6.24 software tool.

2 Implementation facts

Already implemented:

- Hamming errors correction
- Block structure recovering (including sequence and ID mismatch errors)
- 32 bits boundary data alignment (including header positioning)
- RAM write cycles position management (to minimize data bus contention)
- Continuous Blocks Transfer Mode for Merge Mode
- nSTOP signal generation
- Block word counter insertion in highest 16 bits of trailer
- Interlock register feature

Trailer Word Error Bits:

Name	Bit	Implemented	Description
Documented:			
E_CERR	D0	Yes	Correctable Link Error Occurred
E_UERR	D1	Yes	Uncorrectable Link Error Occurred
E_TRUNC	D2	Yes	FIFO is over depth limit (data truncated)
E_BADID	D3	Yes	Event ID Header/Trailer mismatch
E_SHORT	D4	No	FIFO is empty while reading block
E_OVER	D5	Yes	FIFO is full (data truncated)
E_STRUCT	D6	Yes	Block Structure (Sequence) Error
E_ODD	D7	Yes	Odd Link Words in Block Error

Header Word Additional Bits:

I_NCHNL[1..0]	D9, D8	Yes	Channel Number Information (for Merge Mode)
H_UMON	D15	Yes	Update current channel Interlock registers when this block receiving is complete (got trailer)

Special Word (Before Trailer Word):

I_NWORDS[15..0]	D15..D0	Yes	Total Number Of 32-bit Words In Block
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Individual Channel Configuration:

Name	Implemented	Description
CC_ENA	Yes	Channel Enable Enable channel participation in merge mode. Also enable channel participation in GS_Block bit generation.
CC_RXENA	Yes	Link Receiver Enable Enable Link Data Receiving
CC_ECC	Yes	Error Correction Enable
CC_RST	Yes	Reset Channel
CC_MAXBLOCK[15..0]	No	Maximum Block Size

Global Configuration:

Name	Implemented	Description	Comment
GC_CHAIN	No	Chain Mode	
GC_TSTRIP	Yes	Strip Trailer Words	Disable trailer bits modification
GC_32BIT	No	32 Bit Readout Mode	Only 32 Bit Readout supported
GC_ENA	No	Card Enable	
GC_BLOCK	Yes	Block Mode	Enable Word Counter I_NWORDS[15..0] in Trailer
GC_IDMATCH	Yes	Event ID Match Mode	Enable E_BADID bit in trailer
GC_MERGE	Yes	Combine Channel Data	Enable multiple channels by single PCI burst readout.
GC_RST	Yes	Reset All the Channels	
GC_POR	No	Power On Reset	
GC_UMON	Yes	Update Monitoring Registers	This bit clears content of monitoring counters while performing synchronous update of monitoring registers
GC_OVRL[1..0]	New	Set boundary for FIFO_is_Over_Limit condition	While [1..0]=0 limit is 50% While [1..0]=1 limit is 62.5% While [1..0]=2 limit is 75% While [1..0]=3 limit is 87.5%
GC_DAS	New	Set Source for Data_Available[2..0] signals	Those signals are hardwired to PC_MIP connector #3 While GC_DAS=0 Data_Av[2..0]=CS_Block[2..0] While GC_DAS=1 Data_Av[2..0]=CS_Header[2..0]

Individual Channel Status:

Name	Implemented	Description
CS_BLOCK	Yes	FIFO Contains At Least One Complete Block
CS_EMPTY	Yes	FIFO is Empty
CS_FULL	Yes	FIFO is Full
CS_OVER	Yes	FIFO is Over Threshold
CS_HEADER	Yes	Top of FIFO Contains Header

Global Status:

Name	Implemented	Description
GS_BLOCK	Yes	All Enabled FIFOs Contain at Least One Block
GS_EMPTY	Yes	All FIFOs are Empty
GS_FULL	Yes	One Or More FIFO is Full
GS_OVER	Yes	One Or More FIFO is Over Threshold
GS_HEADER	Yes	All FIFO Top Contains Header
GS_TRAILER	New bit	Trailer has been transferred in last single PCI readout cycle
GS_CLOW[1..0]	New bits	Control bits of lower word that have been transferred in last single PCI readout cycle
GS_CHIGH[1..0]	New bits	Control bits of higher word that have been transferred in last single PCI readout cycle

Monitoring Registers:

Name	Implemented	Description	Comments
M_WCOUNT	Yes	Total 32-bit Words Received	25 bit width
M_UERR	Yes	Uncorrectable Link Errors	8+1=9 bit width
M_CERR	Yes	Correctable Link Errors	8+1=9 bit width
M_NBLOCK	Yes	Total Blocks Received	24 bit width
M_SHORT	No	Number Of Missing Trailers	Trailers are inserted automatically by receiver logic to maintain correct block structure
M_TRUNC	No	Number of Block Size Overflows	
M_OVER	Yes	Number of FIFO Depth Limit Overflows	1 bit width
M_FULL	Yes	Number of Times FIFO Was Full	1 bit width
M_OCC	No	FIFO Occupancy	
M_LASTID	No	Last Block ID	
M_BADID	Yes	Number of Block ID Mismatch Errors	8+1=9 bit width

3 PCI memory space

Content from BAR+0000H to BAR+007CH is the same as for PCI configuration space.

BAR+0000H	Configuration/Monitoring Data
BAR+4000H	Channel 0 Data
BAR+5000H	Channel 1 Data
BAR+6000H	Channel 2 Data
BAR+7000H	Merged Data

The meaning of the low 12 PCI address bits is as follows:

AD0..AD7	Event ID
AD8	Block Start
AD9..AD11	Reserved
AD12..AD13	Channel Number/Merged Data Channel
AD14	==0 – Configuration/Monitoring Data ==1 – Channel Data

4 PCI configuration space.

<i>Address</i>	<i>Bits</i>	<i>Read/ write/ hold</i>	<i>Name</i>	<i>Function</i>
4H	1	R/W	mem_en	Enable PCI memory address space
4H	6	R/W	perr_en	Enable Parity Error report on PERR PCI Line
4H	8	R/W	serr_en	Enable System Parity Error report on SERR PCI Line
4H	26..25	R=B"10"	-	Report PCI DEVSEL timing = slow
4H	30	R/W	SSE	PCI Signaled System Error flag
4H	31	R/W	DPE	PCI Detected Parity Error flag
10H	31..15	R/W	BAR	BAR0 Programmable Content

<i>Address</i>	<i>Bits</i>	<i>Read/ write/ hold</i>	<i>Name</i>	<i>Function</i>
40H	1..0	R/W	GC_OVRL[1..0]	Set boundary for FIFO_is_Over_Limit condition While GC_OVRL[1..0]=0 limit is 50% While GC_OVRL [1..0]=1 limit is 62.5% While GC_OVRL [1..0]=2 limit is 75% While GC_OVRL [1..0]=3 limit is 87.5%
40H	2	R/W	GC_TSTRIP	Trailer Strip Mode. Disable generation of error bits in the Trailer.
40H	3	R/W	GC_DAS	Select source for Data_Available[2..0] signals. If GC_DAS=0 Data_Av[2..0]=CS_Block[2..0] If GC_DAS=1 Data_Av[2..0]=CS_Header[2..0]
40H	5	R/W	GC_BLOCK	Block Mode. Enable presence of Word counter I_NWORDS[15..0] in the Trailer.
40H	6	R/W	GC_IDMATCH	Event ID Match Mode. Enable generation of E_BADID error bit in the Trailer.
40H	7	R/W	GC_MERGE	Combine Channel Data Mode. Enable multiple channels data readout by single PCI burst transfer.
40H	8	R/W	GC_RST	Reset all the channels. Same as CC_RST but for all the LRB channels.
40H	9	R/W	GC_AUTOMON	Auto Update Interlock Registers. Content of Monitoring Registers is always transparently passed to PCI bus without holding it in the Interlock registers.
40H	10	R/W	GC_UMON	Update Interlock Register. Enable update of Interlock registers content by value stored in Monitoring registers. Content of Monitoring registers is synchronously cleared at the same time.
40H	12	R/W	GC_SINGLE	Single Word PCI Readout Mode. For testing purposes only. Enable master initiated PCI read cycle terminating. While using this mode content of FIFO can be safely read without PCI burst transfer.
40H	13	R/W	GC_IFIFO	Disable Internal PCI FIFO Overflow control. For testing purposes only. Received data will not be stored in external SRAM due to permanent “not full” status of internal PCI FIFO for storing incoming data.
40H	14	R/W	GC_EFIFO	Disable External FIFO (RAM) Overflow control. For testing purposes only. Received data will be stored in external SRAM without overflow control. Received data will be overwritten by new data as many times as number of received word exceed external SRAM size. This mode might be useful for continuous link reliability testing by checking monitoring registers without performing actual comparison received data against transmitted one.

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<i>Address</i>	<i>Bits</i>	<i>Read/ writ/ hold</i>	<i>Name</i>	<i>Function</i>
40H	16	R/W	CC_RXENA_0	Link Receiver Enable for Channel 0. Enable Receiving of Link Data.
40H	17	R/W	CC_RXENA_1	Link Receiver Enable for Channel 1. Enable Receiving of Link Data.
40H	18	R/W	CC_RXENA_2	Link Receiver Enable for Channel 2. Enable Receiving of Link Data.
40H	19	R/W	CC_ECC_0	Error Correction Enable for Channel 0. Enable Hamming error correction for channel number 0.
40H	20	R/W	CC_ECC_1	Error Correction Enable for Channel 1. Enable Hamming error correction for channel number 1.
40H	21	R/W	CC_ECC_2	Error Correction Enable for Channel 2. Enable Hamming error correction for channel number 2.
40H	24	R/W	CC_RST_0	Reset Channel 0. Reset all relevant to channel 0 FIFO and monitoring registers.
40H	25	R/W	CC_RST_1	Reset Channel 1. Reset all relevant to channel 1 FIFO and monitoring registers.
40H	26	R/W	CC_RST_2	Reset Channel 2. Reset all relevant to channel 2 FIFO and monitoring registers.
40H	27	R/W	CC_ENA_0	Channel 0 Merge Enable. Enable channel participation in merge mode.
40H	28	R/W	CC_ENA_1	Channel 1 Merge Enable. Enable channel participation in merge mode.
40H	29	R/W	CC_ENA_2	Channel 2 Merge Enable. Enable channel participation in merge mode.
44H	0	R	CS_Empty_0	FIFO Empty in Channel 0
44H	1	R	CS_Empty_1	FIFO Empty in Channel 1
44H	2	R	CS_Empty_2	FIFO Empty in Channel 2
44H	3	R	CS_Full_0	FIFO Full in Channel 0
44H	4	R	CS_Full_1	FIFO Full in Channel 1
44H	5	R	CS_Full_2	FIFO Full in Channel 2
44H	8	R	CS_BLOCK_0	FIFO of Channel 0 Contains At Least One Block
44H	9	R	CS_BLOCK_1	FIFO of Channel 1 Contains At Least One Block
44H	10	R	CS_BLOCK_2	FIFO of Channel 2 Contains At Least One Block
44H	11	R	CS_HEADER_0	Top of FIFO of Channel 0 Contains Header
44H	12	R	CS_HEADER_1	Top of FIFO of Channel 1 Contains Header
44H	13	R	CS_HEADER_2	Top of FIFO of Channel 2 Contains Header
44H	14	R	CS_OVER_0	FIFO is over depth limit in Channel 0
44H	15	R	CS_OVER_1	FIFO is over depth limit in Channel 1
44H	16	R	CS_OVER_2	FIFO is over depth limit in Channel 2
44H	20	R	GS_BLOCK	All Enabled FIFOs Contain at Least One Block
44H	21	R	GS_EMPTY	All FIFOs are Empty
44H	22	R	GS_FULL	One or More FIFOs is Full
44H	23	R	GS_HEADER	All FIFO's Tops Contain Header
44H	24	R	GS_OVER	One or more FIFOs is over depth limit

Continued on the next page.

<i>Address</i>	<i>Bits</i>	<i>Read/ write/ hold</i>	<i>Name</i>	<i>Function</i>
44H	28..27	R	GS_CLOW[1..0]	Control bits of lower word that have been transferred in last single PCI readout cycle
44H	30..29	R	GS_CHIGH[1..0]	Control bits of higher word that have been transferred in last single PCI readout cycle
44H	31	R	GS_TRAILER	Trailer has been transferred in last single PCI read cycle
48H	8..0	R/H	M_CERR_0	Number of Correctable Errors in Channel 0
48H	17..9	R/H	M_CERR_1	Number of Correctable Errors in Channel 1
48H	26..18	R/H	M_CERR_2	Number of Correctable Errors in Channel 2
4CH	8..0	R/H	M_UERR_0	Number of Uncorrectable Errors in Channel 0
4CH	17..9	R/H	M_UERR_1	Number of Uncorrectable Errors in Channel 1
4CH	26..18	R/H	M_UERR_2	Number of Uncorrectable Errors in Channel 2
50H	8..0	R/H	M_BADID_0	Block ID Mismatch Errors in Channel 0
50H	17..9	R/H	M_BADID_1	Block ID Mismatch Errors in Channel 1
50H	26..18	R/H	M_BADID_2	Block ID Mismatch Errors in Channel 2
54H	24..0	R/H	M_WCOUNT_0	Total 32-bit Words Received in Channel 0
58H	24..0	R/H	M_WCOUNT_1	Total 32-bit Words Received in Channel 1
5CH	24..0	R/H	M_WCOUNT_2	Total 32-bit Words Received in Channel 2
60H	23..0	R/H	M_NBLOCK_0	Total Blocks Received in Channel 0
64H	23..0	R/H	M_NBLOCK_1	Total Blocks Received in Channel 1
68H	23..0	R/H	M_NBLOCK_2	Total Blocks Received in Channel 2
6CH	0	R/H	M_FULL_0	FIFO_Full condition has been detected at least once in Channel 0
6CH	1	R/H	M_FULL_1	FIFO_Full condition has been detected at least once in Channel 1
6CH	2	R/H	M_FULL_2	FIFO_Full condition has been detected at least once in Channel 2
6CH	3	R/H	M_OVER_0	FIFO_is_over_depth_limit condition has been detected at least once in Channel 0
6CH	4	R/H	M_OVER_1	FIFO_is_over_depth_limit condition has been detected at least once in Channel 1
6CH	5	R/H	M_OVER_2	FIFO_is_over_depth_limit condition has been detected at least once in Channel 2

Note.

Access mode “Hold” means that those data are stored in Interlock Register and should be read out by using access method defined for Interlock Register operations.