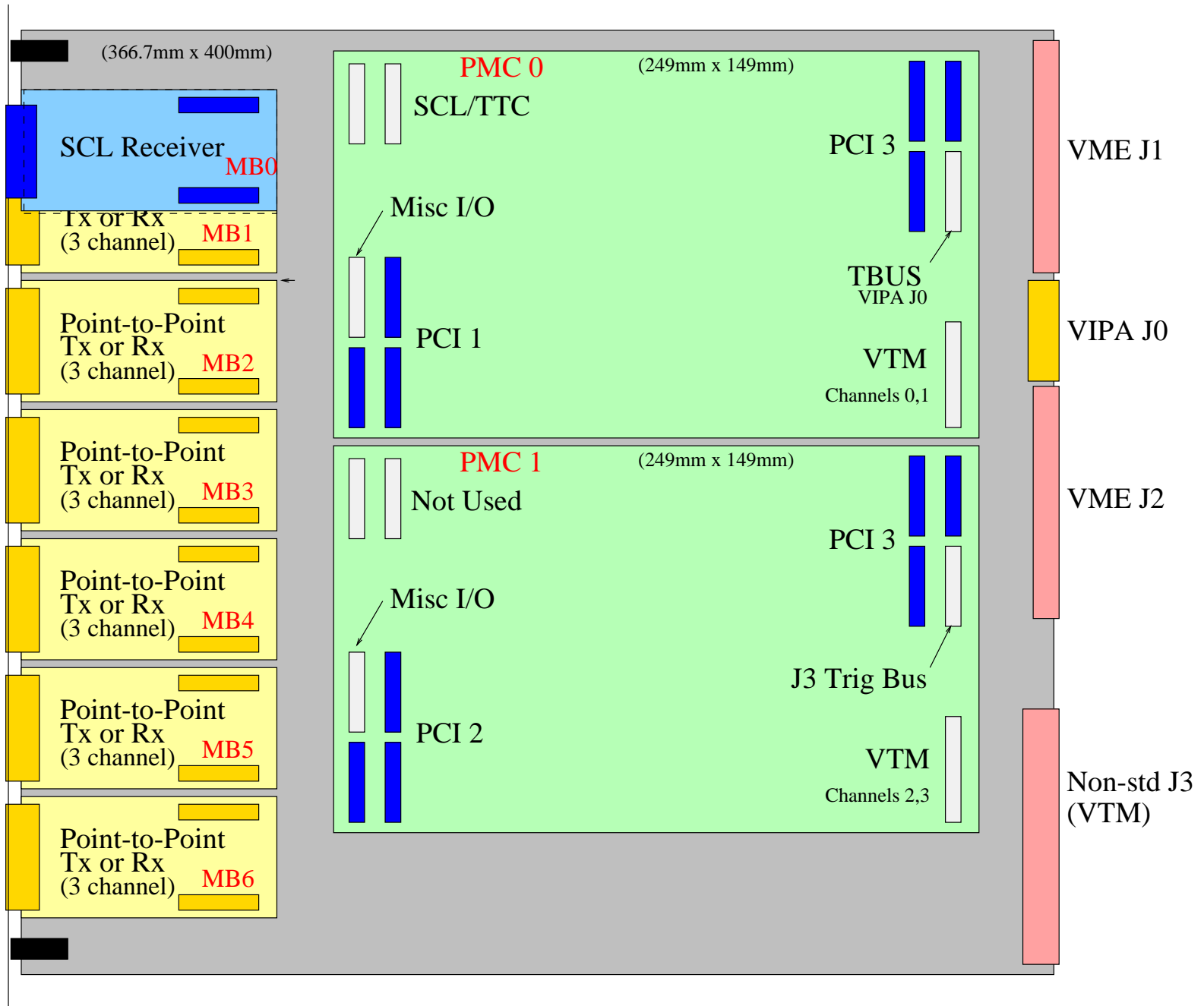




9U Motherboard Layout

Boston University



Specification is Converging:

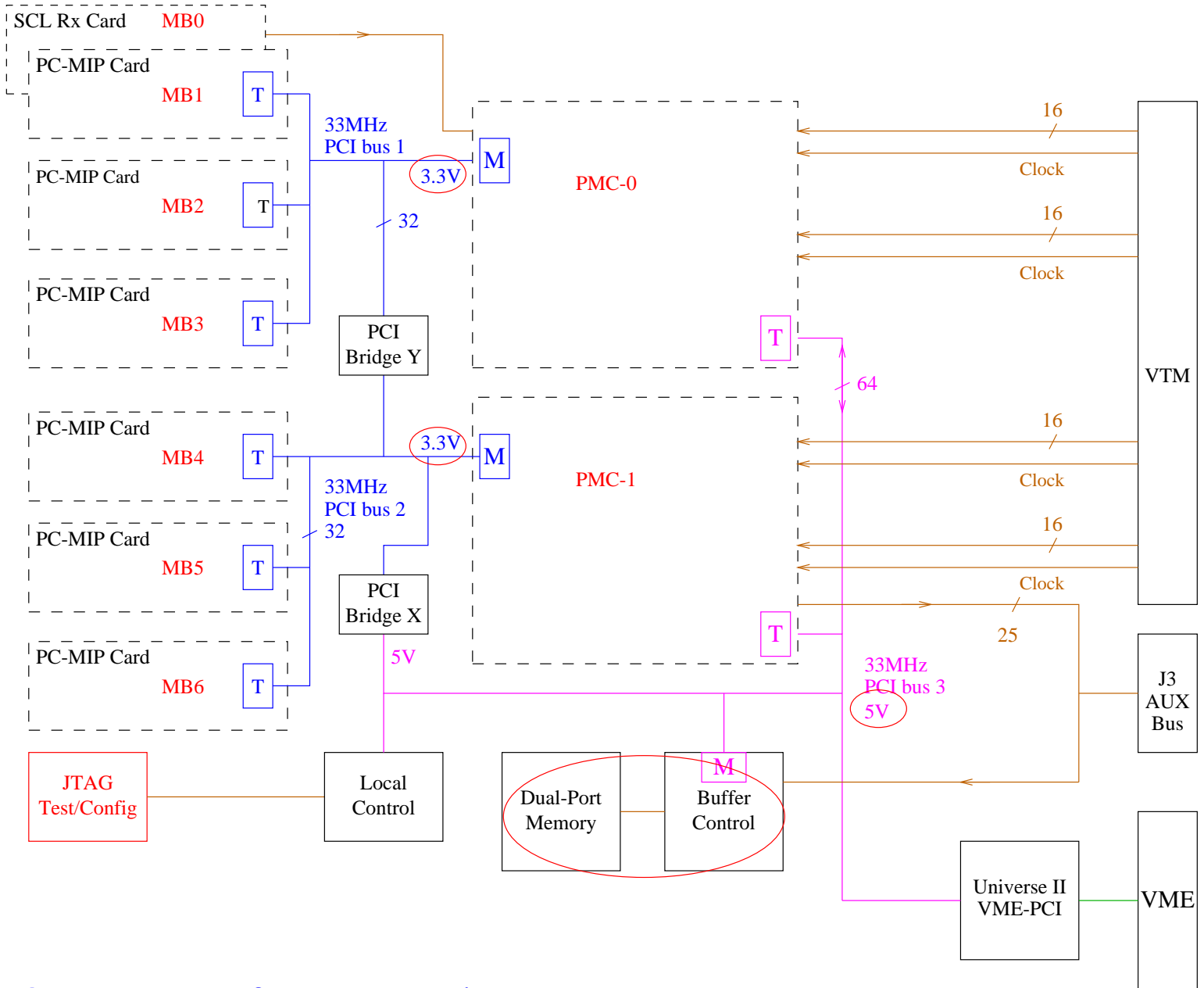
Placement of connectors / mezzanine boards is ~fixed

Basic functionality is understood

Spec document with pinouts of connectors, etc exists



9U VME Motherboard Block Diagram



Open Issues for MB Design:

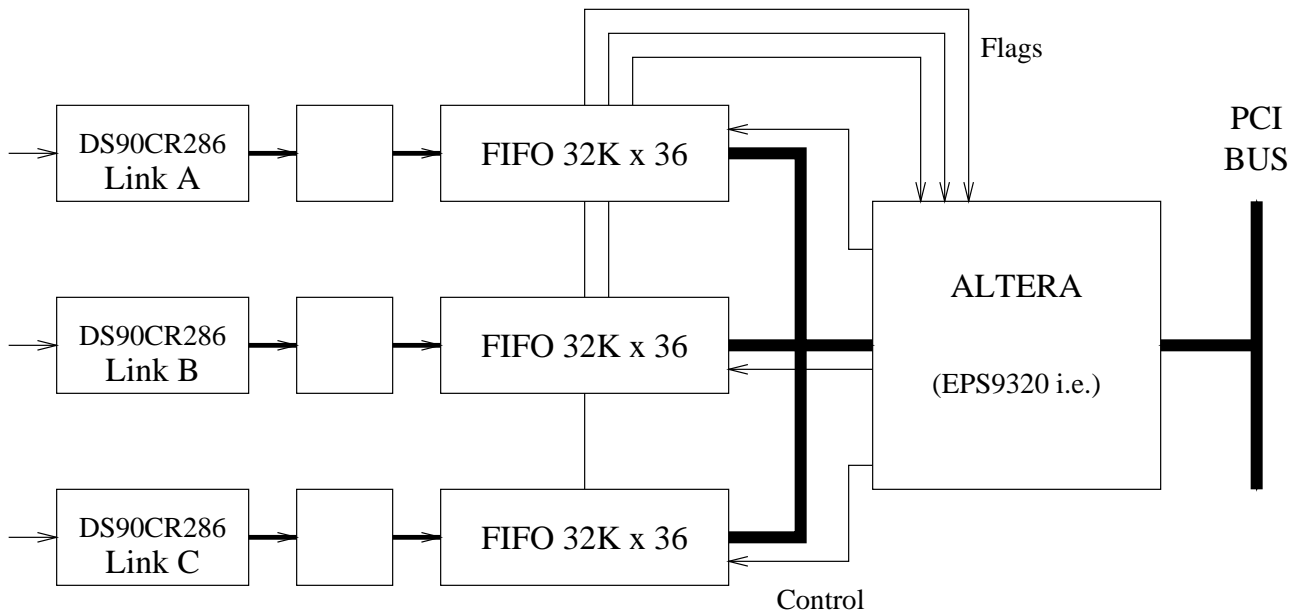
PCI Bus voltages: currently mixed 3.3/5V

Details of buffer control logic (Columbia)

Power supplies (fusing, distribution)



Link Receiver Board



PC-MIP Link Receiver Block Diagram

S2	S1	Byte 1	Byte 2	State
1	1	Reserved	Event ID	<i>Header</i>
1	0	User Data	User Data	<i>Data</i>
0	1	Error Flags	Event ID	<i>Trailer</i>
0	0	0	0	<i>Idle</i>

Data Format



D0 STT Engineering Meeting

E. Hazen - 28 Jan 2000

Point-to-Point Link Status

Design of receiver is underway. Details subject to change as design proceeds.

Fixed features in the LRB design:

- o 16 bit data path (packed by two in 32-bit words on PCI bus)
- o Hamming code error-correction to correct single bit errors
- o Block structure encoded in link (header, data, trailer)
- o 8-bit "Event ID" in header and trailer; match checked at receiver
- o Single PCI block read for entire event across multiple links
- o On-board monitoring registers
- o Hard-wire status signals to PMC site (for handshaking)

Transmitter design will be done after receiver is completed.

Important transmitter features:

- o One common transmitter FIFO feeds 3 link transmitters
- o Single PCI block write for entire data block
- o Diagnostic mode for repetitive pattern transmission