



Review of L2STT

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PC-MIP Link Receiver Board

Implementation Details

PC-MIP (PCI bus Module Industry-Pack) standard chosen
provides 32 bit PCI bus interface in convenient format

Receiver buffer in 36-bit FIFO (sizes 1k-128k available)

All logic in a single Altera MAX9000 fast FPGA

Extensive error correction/recovery/monitoring built in

Current Status and Plans

Engineering design now underway - complete by 3/3/00
(PCB design, FPGA program)

Prototypes expected by 3/24/00