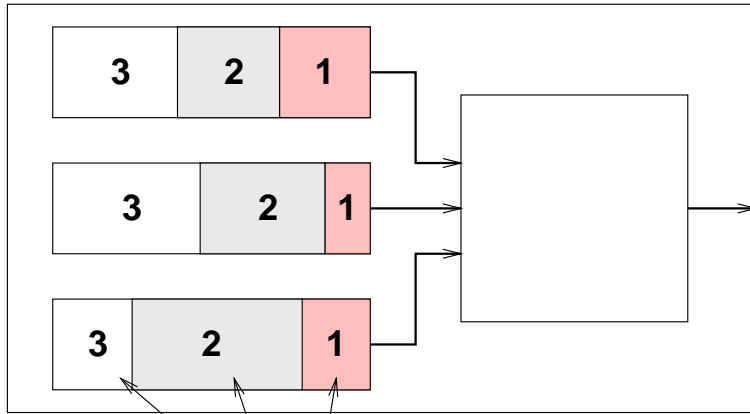




PC-MIP Link Receiver Board

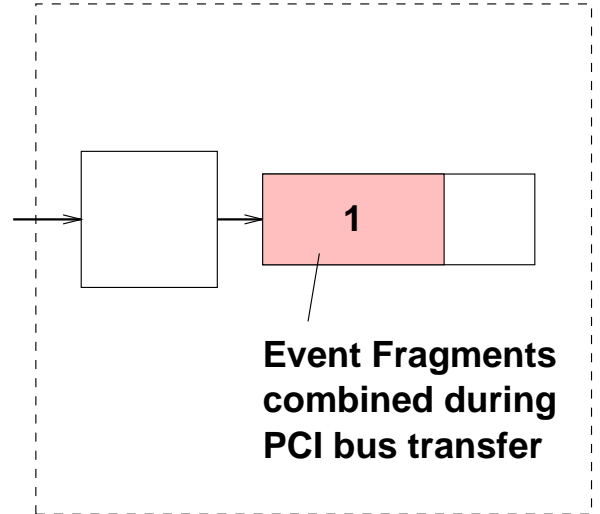
Event-Building Functions

Link Receiver Board(s)



Event Fragments

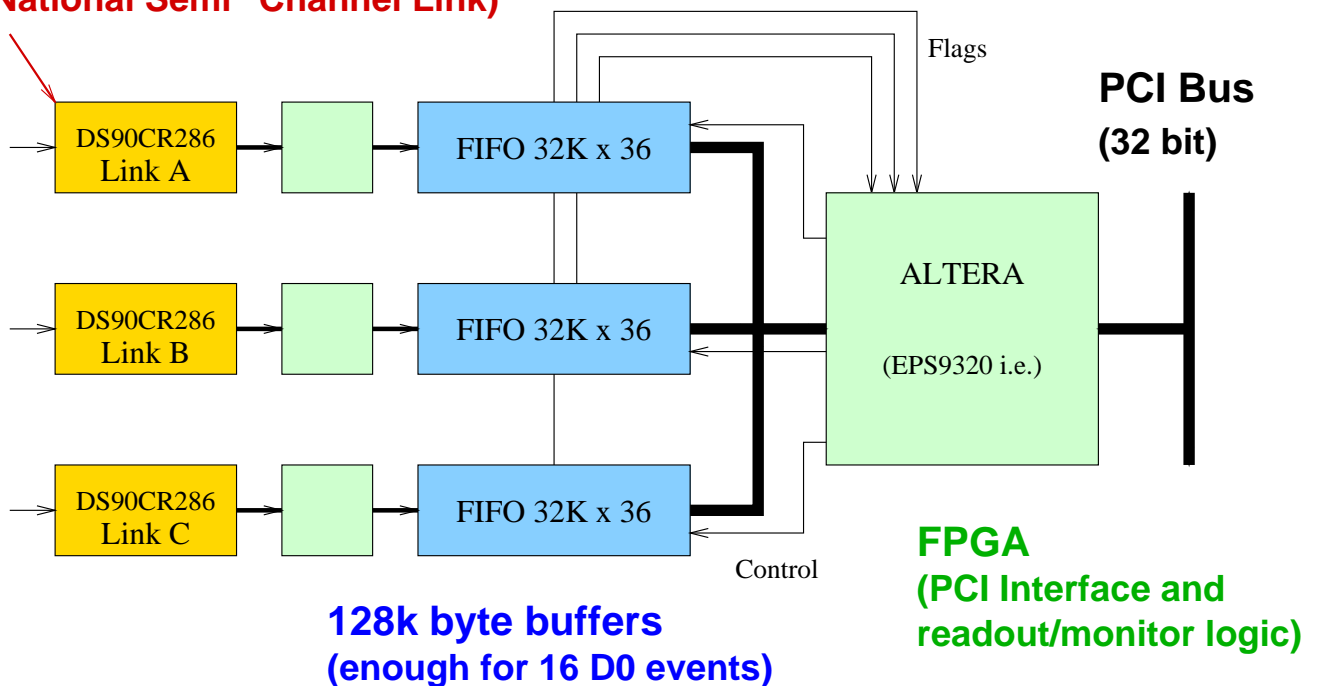
Logic Board



Event Fragments combined during PCI bus transfer

Block Diagram

LVDS Serial Receivers (i.e. National Semi "Channel Link")



128k byte buffers (enough for 16 D0 events)

FPGA (PCI Interface and readout/monitor logic)