



Initialization of STT Components

Condensed from FRC document. Hal will update and distribute more detailed info soon...

1. Power-Up Reset (signalled by VMEbus SYSRESET)

Hardware reset sequence:

- Reset all synchronous logic to known state
- Reload FPGAs from flash/EEPROM if required

VME CPU performs the following actions:

- Configure PCI busses
- Power-up tests (check for presence of boards, memory, etc)
- Set PCI addresses on mezzanine boards where required
- Download LUTs

2. SCL_INIT (must complete in ~ 1ms)

Receive RESET command via PCI bus (bit set in CR)

Input element reset:

- Disable latching of input data
- Wait n clock cycles with no valid data from input
- Enable latching of input data

Processing element reset:

- Reset FIFOs
- Reset synchronous logic to known 'ready' state

Acknowledge READY via PCI bus (bit set in SR)

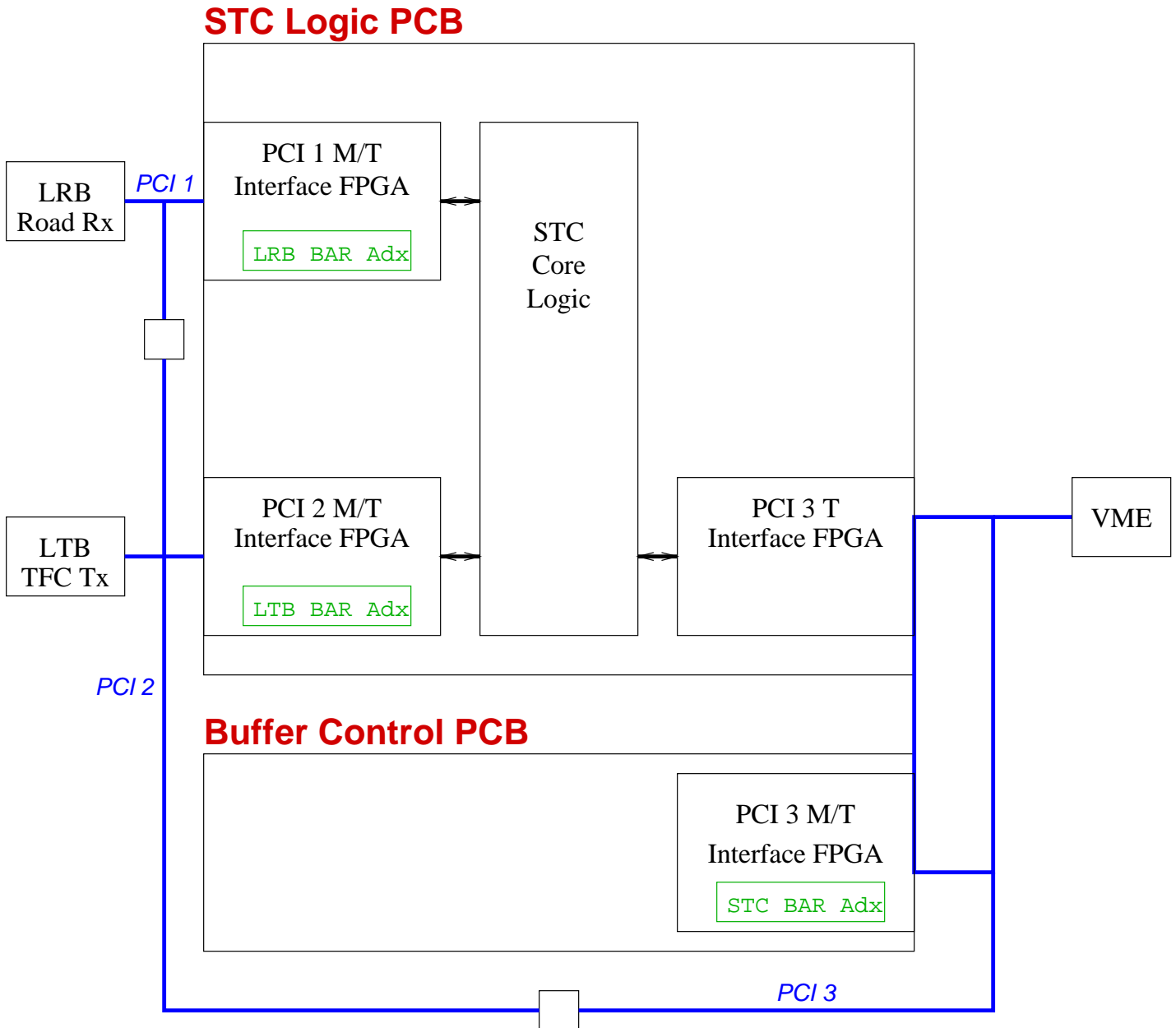


Boston University

D0 STC Engineering Meeting

E. Hazen - 21/22 Apr 2000
Boston University

More STC PCI Initialization Details



Each PCI master interface needs to know the base address of at least one target. These will be set by the CPU during PCI configuration.