



DCC PCI 1/2 Registers



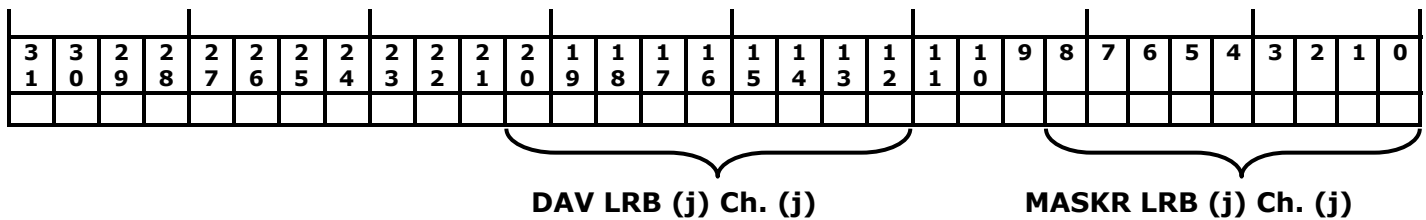
- BARO + 00h -** LRB1 Address Register Ch1. Write/Read
- BARO + 10h -** LRB1 Address Register Ch2. Read
- BARO + 20h -** LRB1 Address Register Ch3. Read

- BARO + 04h -** LRB2 Address Register Ch1. Write/Read
- BARO + 14h -** LRB2 Address Register Ch2. Read
- BARO + 24h -** LRB2 Address Register Ch3. Read

- BARO + 08h -** LRB3 Address Register Ch1. Write/Read
- BARO + 18h -** LRB3 Address Register Ch2. Read
- BARO + 28h -** LRB3 Address Register Ch3. Read

- BARO + 0Ch -** Test and Mask Register
- BARO + 1Ch -** Test Data FIFO

Test and Mask Register



<u>BIT</u>	<u>TYPE</u>	<u>Description</u>	<u>Active/Valid = "1"</u>
31	R	- Data Buffer FIFO Full Flag	
30	R	- Data Buffer FIFO Empty Flag	
29	R	- Select 32/16 Multiplexed Data FIFO	
28	R	- Read FIFO REQUEST	
27	R	- Test FIFO Full Flag	
26	R	- Test FIFO Empty Flag	
25	R/W	- Test FIFO Write Enable	
24	R	- Reserved	
23	R	- Trailer to DCC (<i>CTL2</i>)	
22	R	- Header to DCC (<i>CTL1</i>)	
21	R	- Data Valid to DCC (<i>CTL0</i>)	
20...12	R	- Data Available	8...0 R/W - Mask Register Value
		20 - LRB3 Ch.3	8 - LRB3 Ch.3
		19 - LRB3 Ch.2	7 - LRB3 Ch.2
		18 - LRB3 Ch.1	6 - LRB3 Ch.1
		17 - LRB2 Ch.3	5 - LRB2 Ch.3
		16 - LRB2 Ch.2	4 - LRB2 Ch.2
		15 - LRB2 Ch.1	3 - LRB2 Ch.1
		14 - LRB1 Ch.3	2 - LRB1 Ch.3
		13 - LRB1 Ch.2	1 - LRB1 Ch.2
		12 - LRB1 Ch.1	0 - LRB1 Ch.1
11...10	R	- Reserved	
9	R	- DCC Buffer Full (<i>CTL3</i>)	