DHCAL Back-End

Eric Hazen,
John Butler, Shouxiang Wu

Boston University
DCOL Status

- 3 Boards Stuffed - hardware tested and working
- Preliminary firmware released
- Testing underway at ANL and Boston
- Still missing:
  - Current-limiting chips for front-end links
  - Front panels
Firmware Status

• What is still missing
  - Only “Circular buffer mode” implemented
  - No sorting by timestamp
  - No monitoring counters
    • We should specify what we want!

• What has been tested (superficially)
  - SDRAM memory test
  - Flash programming from VME
  - Front-end link
    • Slow control write/read
    • Hit data read
Next Steps - Hardware

- Reproduce BU link tests at ANL
- Further link tests with Xilinx board
- Integrate DCOL with DCON
- Integrate DCOL with TTM
- Update/fix DCOL firmware as needed