DHCAL Back-End

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DCOL Status

- PCB due back today.
  Stuffed PCBs due 4/6 (or sooner)
- VME Interface Defined
  - Firmware development underway
  - First version should be ready with PCBs
- Link Tester built - simple tests of front-end link working
TTM Input

Front-End Links

Current-Limited 5VDC to Front-End Links

Address Switches

Spartan 3E FPGA
DCOL Readout Modes

“Page Mode” - Fixed 16k buffers, each with one timestamp

“Circular Buffer Mode” - one continuous buffer with hits in time order

VME BLT of up to 16k (all hits with one timestamp)

Groups of hits with matching timestamps

VME BLT of any size (up to 24MByte)
DCOL Readout Modes

- VME Operations to Read DCOL
  - Page Mode - readout actions per DCOL
    - Read Event_size (byte count) for next buffer
    - VME BLT for Event_size bytes
    - Write to MEM_PAGE to advance to next buffer
  - Circular Buffer Mode
    - Read Event_wp and Event_rp (buffer pointers)
    - VME BLT all available data

- Choice depends on software considerations
FE Link Tester

Xilinx Spartan 3E Evaluation Board

FE Link Daughter Board

Isolator

LVDS Transceivers
Plans

- Setup VME Crate and Bridge
  - (will likely use CMS setup for initial checkout)
- Test basic DCOL functionality with stand-alone C software
- Ship DCOL#2 to ANL as soon as it shows signs of life
- Coordinate further testing with DAQ guys
Backup Slides
Readout Overview

Front-end Link:
- 10Mhz clock
- Triggers
- Test pulse
- Slow control
- Hit Data