Some preliminary ideas after workshop with Gary Drake

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DHCAL Readout
(one plane shown)

- Front-End Boards
- Kapton Cables
- Data Concentrator
- Ribbon Cable
- Data/Super Concentrator
- Data Collector
- Trigger Timing Module
- VME Crate

Details may change!
Data Collector (DCOL)

- **SERDES buffering**
- **FPGA**
  - **Spartan 3E** (2 required)
- **SDRAM** (if needed)
- **Event Builder, VME64**
- **CPLD**
- **JTAG**
- **LVDS**
- **RJ-45**
- **Total of 12 I/O cables**
- **Trigger, Timing input**
- **Low-skew fanout of clock, trigger, timing**
- **5V Buffers**
- **VME**
Proposed Link Technology

Super-Concentrator

Capacititative or GMR Digital Isolator

Shielded Twisted Pair Cable (4 pairs)

Data Collector

FPGA (Spartan-3E)

LVDS

Power to far end

Separated power/GND plane for isolated electronics (powered from DCOL end)
Data Encoding
(one possible scheme)

Rising edges occur at steady 40MHz rate
Bit encoding by pulse width

First bit always '1', pattern '1000' used for synchronization

This type of code would be easy to implement in a Xilinx FPGA
DLL (delay-locked loop) in FPGA would recover clock with ~0 skew
Delayed clock output would sample bits to recover data stream
Return Data
(from Super-Concentrator to Data Collector)

100ns Frame

1 0 0 0 0 1 1 0 0

- Start Bit
- DAQ data 0
- DAQ data 1
- Slow Control Data

Remaining 3 bits used to send data at 10Mbit/sec

For data readout, two bits could be assigned to provide 20Mbits/sec.

If more bandwidth is required, a clock rate higher than 40MHz could be used.
DCOL Front Panel

Space is available for 12+1 RJ-45 connectors on a 6U panel (using quad shielded connectors)

12 inputs for super-concentrators

1 input from master trigger/timing module
Next Steps

- Define higher-level protocols:
  - Slow Control
  - Data Readout
  - VME Access

- Write specifications or some sort of description for:
  - Front-end board
  - Data/Super Concentrator
  - Data Collector
  - Timing/Trigger module