New DCC Overview

- Single board; 15 HTR spigots, Ethernet, TTC, TTS on front
- Optional P3 rear transition module for *i.e.* future selective readout

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**Xilinx XC3S200A FPGA**
- 32MByte DDR SDRAM

**Xilinx XC3SD1800A FPGA**
- TP Out / Readout bits in
- DAQ Data
- LVDS Tx
- TTC
- TTCrx UMD board
- 64MByte DDR SDRAM

**TTCrx UM board**
- Ethernet (WizNet)
- RJ-45 (WizNet)
- RJ-45

**VME Buffers**

**VME64x**

**Optional rear transition module**

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2008-12-09

E. Hazen

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New DCC

- Ethernet
- TTC
- TTS
- Slink (back side)
- 3 HTR Inputs
- Event Builder
- VME64 Interface
- TM Connector (future opt.)
Update from Wu this morning:

Eric,
As of now, all seven FPGAs can be configured from the SPI FLASH at power up or upon VME commands. Three configuration data CRCs (VME, LRB and main chip) are correctly calculated during configuration. The links between the chips are all working. The monitor buffer memory attached to the main chip is working correctly as far as VME read/write can tell. LRB registers can be written/read back through VME correctly. At the moment, I'm working on the LRB SDRAM event buffer memory VME access.

Shouxiang
Test Plan

- Thorough testing at BU  
  - 100kHz or higher random trigger rate, with 12 HTR inputs operating (simulated data)
  - TTS backpressure test
  - S-Link Receiver
  - Full xDAQ software

- Tests at CERN in 904  
  - March – April
  - Validate BU results
  - Test with real front-end data from test RBX

- Tests in USC55
  - Take local and global data; validate 904 results
  - Mostly software validation, we hope!

- Production not yet authorized, but will cost about $42k