New DCC Status and Plans

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Introduction

- Why a new DCC?  Some justification and history
- Comparison of old and new designs
- Current status
- Plan for commissioning and test of new DCC
Old DCC – 1999 Design

- Based on D0/STT design
- It has generally worked well
  - Running since 2001 source test
- Hardware now difficult to maintain
  - 10 daughter-boards
  - 10+ firmwares
  - Too many chips and connectors
- Inadequate performance
  - < 200 MB/sec absolute transfer rate limit (internal design bottleneck)
Old DCC Status / History

- Goal – a module which is robust and simple to maintain available before LHC startup, with generous spares

- Old DCC Status:
  - 3 working spares, but there are still outstanding needs (for CASTOR, etc). Some modules at BU and CERN with problems
  - Often ”repair” is a matter of re-seating all connectors, reprogramming firmware and other unsatisfactory voodoo

- Some history...
  - Replacement was proposed first in 2004 before final production, but the plan was rejected based on 2007 LHC startup schedule
  - Proposed again in Feb '08 but tabled
  - Final approval to go ahead with prototypes only in Fall 2008
Old vs New

Old DCC
Base design done in 1999 for D0/STT
Assembly of 10 PC boards
10 Firmware designs (by 4 designers!)
~ 3k mated contact pairs
Many components obsolete

New DCC
Designed from scratch in 2008
One PC board (plus TTC, SLink)
3 Firmware designs (by 1 designer)
~ 250 mated contact pairs
All components available from stock
New DCC Overview

- Single board; 15 HTR spigots, Ethernet, TTC, TTS on front
- Optional P3 rear transition module for *i.e.* future selective readout
New DCC

- Ethernet
- TTC
- TTS
- Slink (back side)
- 3 HTR Inputs
- Event Builder
- VME64 Interface
- TM Connector (future opt.)
New DCC Features / Fixes

- Ethernet interface for diagnostics independent of state of DAQ
- Much higher internal bandwidth
  - Could easily accommodate non-ZS input data and perform ZS or selective readout on DCC if desired
- Much simpler internal protocols (no PCI)
  - Firmware should be more straightforward and easier to maintain
- Sufficient bypass capacitors for full utilization of FPGA resources if needed
10 Prototypes assembled

Initial testing completed... no hardware problems so far

Firmware development underway

Expect to be ready for CERN tests by mid-March (conservative)

Software work going on in parallel
Goal: plug-compatible with old DCC
- One crate may contain both old and new DCC!

How to manage this?
- Current hcalDCC class becomes a wrapper
- DCC1 and DCC2 classes represent old/new boards
- All current methods will exist at least as stubs

Strategy
- Add new classes to CVS very soon so new releases will have this structure to avoid divergent code
- Add functionality to DCC2 class as it is developed

Who will do it?
- Phil, Eric, Arno
Software Issues

- Firmware programming – different set of files
  - Firmware DB will need some updating
  - Benefits: Everything is reprogrammable, much faster
  - Jeremy says this is easy to support
- MonLogger
  - Many counters expand from 8 to 32 bits
  - Some totally new items
  - Some old items disappear
  - Update monitoring DB schema to be superset of both
- HyperDAQ Expert View
  - Same issues as monlogger
Test Plan

- **Thorough testing at BU** Now - mid-March
  - 100kHz or higher random trigger rate, with 12 HTR inputs operating (simulated data)
  - TTS backpressure test
  - S-Link Receiver
  - Full xDAQ software

- **Tests at CERN in 904** March – April
  - Validate BU results
  - Test with real front-end data from test RBX

- **Tests in USC55**
  - Take local and global data; validate 904 results
  - Mostly software validation, we hope!

- Production not yet authorized, but will cost about $42k