HCAL DAQ / Timing / Controls Module

Eric Hazen, Shouxiang Wu

Boston University
DTC Requirements

- **Clock / Controls**
  - Receive TTC and/or upgraded controls stream
  - Distribute clock and synchronous controls

- **DAQ**
  - Readout DAQ data, optionally perform ZS or SR
  - Transmit to SLink (via adapter) and/or new DAQ

- Must be an MCH card for connectivity
- Could eventually perform minimal MCH functions
Existing HCAL Crate
(complex cable plant!)

- Front-end Fibers (8x)
  Total 48 ch/HTR

- CAEN VME Bridge

- HTR VME Module

- HTR to DCC LVDS serial

- TP to RCT Vitesse serial

- DCC VME Module

- SLink-64

- TTC fanout VME Module

- TTC/clocks

- Vitesse serial

- TTC/clocks

- SLink-64

- VME Module
MicroTCA HCAL Crate

- 18 Links per SuperHTR
- GOL or GBT
- Ethernet
- TTC (Legacy) or new control/timing link
- Optical Trigger Links
- Adapter (VME?)

- TTS
- SLINK-64 (multiple)
Vadatech VT891 - commercial uTCA crate

MCH1 (commercial): Ethernet, management interface

MCH2 (DTC): Clock/controls distribution, DAQ
MCH Mechanics (in progress)

Front panel space very tight!
Barely room for 3 SFP+ and TTC receiver

MCH requires 4 connectors
Plan is to use 2 PCBs, with connectors only at other two sites.
DTC Clock / Controls PCB

- TTC Fiber Rx
- Clock Recovery
- Q PLL
- Alternate Clock
- Low Skew Clock Fanout
- AMC 1
- AMC 2
- AMC 12
- Spartan Class FPGA
- Clocks to MCH connector 2
- Serial controls to MCH connector 1 (fabric A)

Fast Controls stream from DAQ PCB
DTC DAQ board

DAQ fiber
Ethernet fiber
Spare fiber

Clock / Controls from Clock PCB

Virtex 5/6 FPGA

Fabric D to AMC 1-12
Fabric E to AMC 1-12

MCH Connector 3 (4)

~ 6Gb

DAQ
Spare

DAQ fiber
Ethernet fiber
Spare fiber

Clock / Controls from Clock PCB

Virtex 5/6 FPGA

Fabric D to AMC 1-12
Fabric E to AMC 1-12

MCH Connector 3 (4)

~ 6Gb

DAQ
Spare
Management

- Should this be a full-function MCH?
  - This implies a GbE switch (or a huge FPGA)
  - Probably will not include this HW on first prototype
- Must include IPMI interface and 2 GbE ports
- Expect to piggyback on other efforts...
Status and Plans

- Goal - Test beam summer 2010 with uTCA system!
- Good news: some FY10 funding
- SuperHTR / miniCTR2 card built at Minnesota and under test
- uTCA test crates available at BU, MN
  - But, need dual-start crate and MCH for DTC testing
- Detailed design just starting for DTC
Spare Slides
**DTC Board Stack**

- **Build boards 1, 2 first**
  - Board 1: Power, controls
  - Board 2: Clocks
- **Build boards 3, 4 second**
  - DAQ concentrator

The diagram illustrates the board stack layout with labeled components:
- **MCH Slot**
- **Backplane connectors**
- **Board-to-board Connectors**
- **Virtex 5/6 Class FPGA (MGTs)**
- **Heatsink**
- **Optical Transceiver (DAQ / Fast controls)**
- **Front Panel**
  - Power, Ethernet, I2C, Fabric Port A
  - Clocks
  - Fabric Ports D, E, F, G
Typical 12-Slot MicroTCA Backplane

(Schroff)