Senior Design

ENG EC 464

Memo

To: Professor Pisano, Professor Kia, EC 464 Staff

From: Caroline Ekchian, Benjamin Havey, Andy Mo, Thomas Nadovich and Christopher Woodall

Team: Team #19: Team dDOSI

Date: 4/24/2014

Subject: Functional Test Report

1 Test Overview

In this test we tested our integrated hardware and software, which included two PCBs (the motherboard and the DDS frequency synthesis module), the microzed firmware and server, and the Windows GUI and client code for interacting with the device. The test took place in the customer's lab in ERB B05 with a full optical test on an optical phantom with known characteristics. The data from this test was used to analyze our systems accuracy compared to pre-existing systems. The test itself involved setup, data collection, and data analysis to prove functionality and performance.

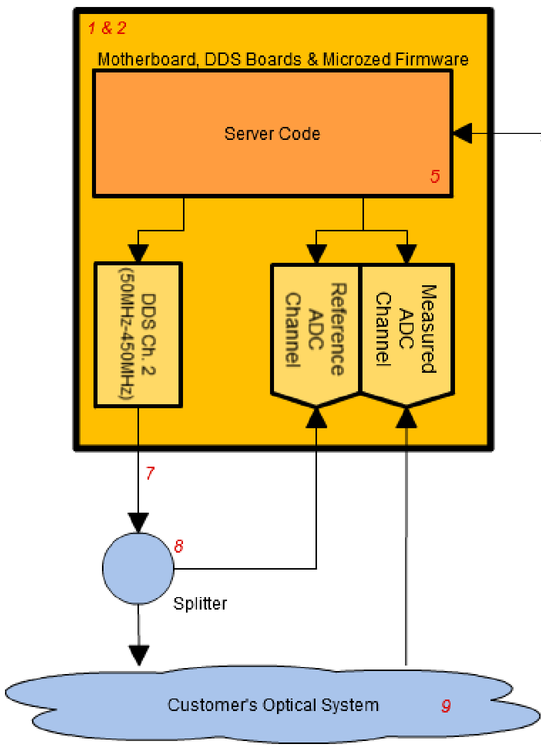
This was the first full system test which included both the hardware and software integrated into one usable package. This test had two major goals, one of them was to test the functionality and compatibility with the current system, the second was to test the performance of the device as used in system compared to previous measurement devices used by our customer. This test proved that our system met many of our fundamental requirements that are listed in *Section 1.1* of the test plan. Additionally, it showed that our system has performance that is comparable to that of prior systems.

2 Equipment and Setup

2.1 Setup

The setup for our test is presented in *Figure 1*. The goal of this setup was to provide a functional test on a known working optical phantom. This test was constructed in this way so that the data retrieved could be analysed by the researchers and compared with the previous systems.

Figure 1: Diagram of Test



Our system, shown in Figure 1, consisted of our two PCB's and the MicroZed, attached to a laptop running Windows 7 which hosts our user facing client code. On the GUI, a profile containing information for the sweep (e.g. start frequency, step size, number of parameters, etc) was set up. This information is sent to the server code running on the MicroZed, which then starts a sweep. The output of our DDS drive the input of a splitter which splits the signal to our reference ADC channel (CH. B) and the laser diode driver. After the sweep is done a *.csv* file with the unprocessed time domain data is ready for analysis.

2.2 Equipment

The following equipment was used

1. Motherboard PCB fully assembled, with MicroZed installed

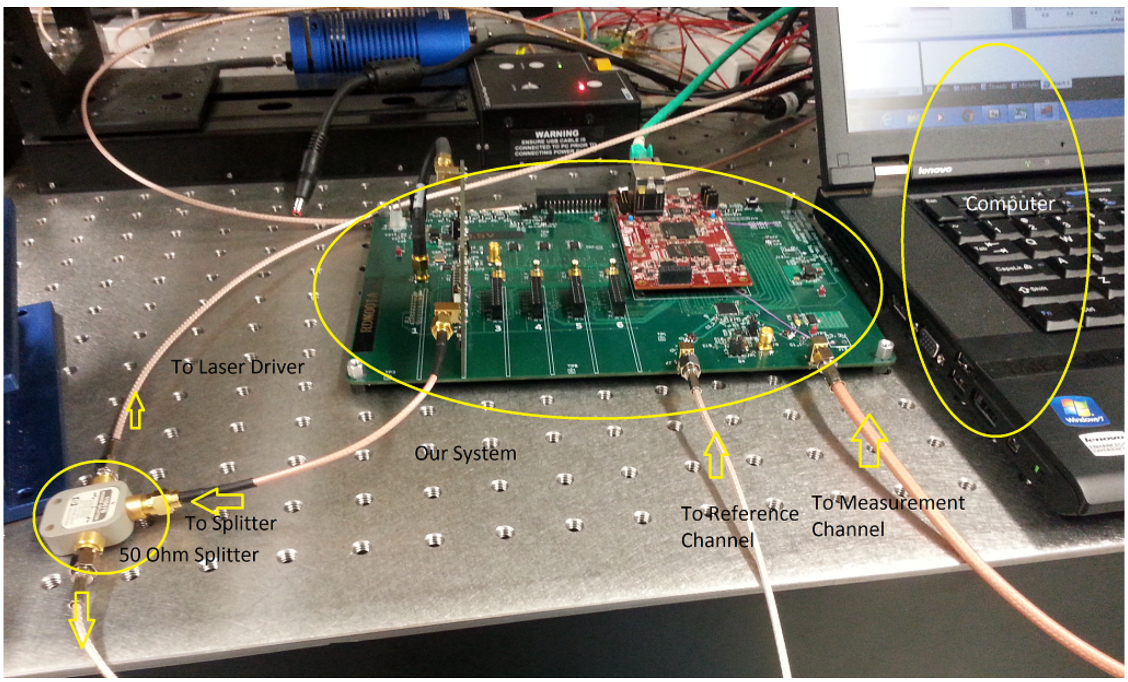
2. DDS PCB fully assembled
3. Cat6 Ethernet Cable (1000Mbps)
4. Windows Executable for Client GUI
5. Server Code on SD Card for Microzed (includes FPGA .bit file)
6. Windows 7 Laptop with 1000Mbps Ethernet Link
7. 4 SMA cables for use with Darren's System
8. Splitter to generate reference and drive signal from DDS output

9. The optical phantom we are testing against

Additionally, 120VAC wall power was used to power the 5V AC-DC switching power supply that provides power to our system. The wall power was also used to power the rest of our customer's system. That system was composed of the following:

- An RF switch
- A laser diode driver
- An optical phantom with known characteristics
- An avalanche photodiode detector (with temperature compensation electronics)
- A broadband 40dB "gain block" amplifier (~10MHz-700MHz bandwidth)
- A computer for controlling the system

Figure 2: Picture of setup (with labels).



3 Measurements

3.1 Measurement Procedures

Our functional test was done in two stages. For the first stage, the baseline for the noise floor was measured by running the system at different sample sizes without ADC input. Once the baseline was obtained, ADC Channel B was connected to the reference source and ADC Channel A was connected to the return signal coming from the amplifier board (Figure 1 and Figure 2). A total of four different profiles (each with different start frequency, step size, sample size, and number of steps), were then run three times each.

3.2 Profiles Used For the Test

Table 1: Profiles with Relevant Settings

	Start Frequency (MHZ)	Step Size (MHz)	# of Steps	Sample Size (kS)
Profile 0	50	1	400	4
Profile 1	50	1	400	8
Profile 2	50	10	40	4
Profile 3	50	1	1	4

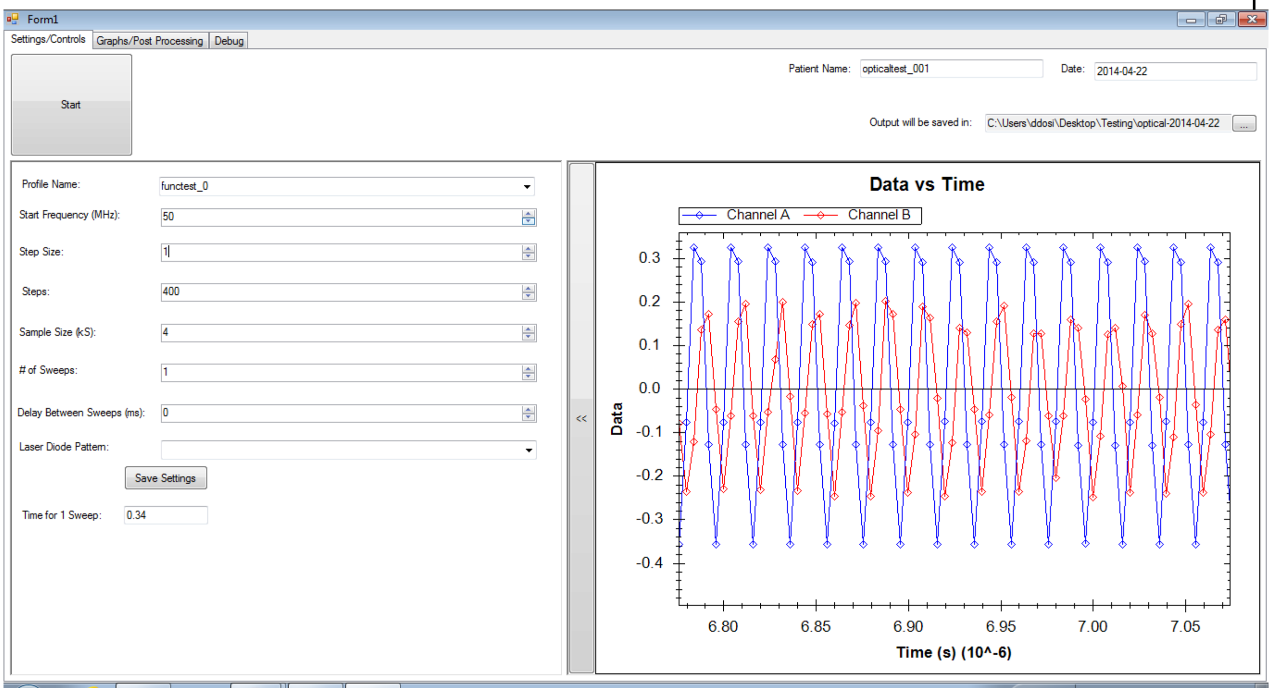
In *Table 1* the profiles under test are listed, each profile serves a purpose:

- Profile 0: Nominal case.
- Profile 1: Worst Case.
- Profile 2: A "fast" test, this may be used for obtaining multiple sweeps in a heartbeat, where granularity of the sweep is less important than the time domain information.
- Profile 3: Single transfer, used for overhead analysis.

Each of these profiles were run 3 times to gather adequate data for analysis.

The data collected included frequency domain information from the ADC and throughput performance information from the GUI. This information was collected by first setting up a run profile on the GUI followed by clicking start. This action was all that was required due to the automation of the data collection and performance calculations done by the GUI and related libraries. Multiple tests using the profiles listed in section 3.2 were run to gain additional information for analysis on data accuracy and throughput speed. The data obtained from these tests were stored as sets of ".csv" files, which were later input into numeric analysis packages for assessment. A successful run is shown in *Figure 3*.

Figure 3: Graphical User Interface after Successful Test Run



4 Assessment of Measurements

5.1 Criteria for Success

A successful test will include the following:

- Our hardware component successfully interfacing with the optical system we are measuring and stimulating.
- Our software successfully communicating with our hardware and returning meaningful data in the quantities, sizes, etc. which we specified.
- A transfer of 4kSamples/step at 400 steps takes less than 1 second.
- A reasonable looking frequency domain response with a peak at the desired frequencies and minimal noise.

4.2 Ethernet and Software Performance and Functionality

We analyzed the data of 30 tests for each profile and recorded the mean time and standard deviation of the run times to figure out what our transfer performance was. Furthermore, we also calculated a transfer rate from the mean time and the profile parameters. The results are shown in *Table 1.* The variable transfer rates at different speeds are in part due to the amount of data we are sending, but the *Profile 0* and *Profile 1* cases are useful for determining our actual throughput and efficiency over our ethernet link. *Profile 2* and *Profile 3* show us a little bit about our overhead.

Table 1: Ethernet Transfer Time

Profile Name	Mean Time (s)	Standard Deviation	Throughput (Mbps)
Profile 0	0.3359	0.0027	156.0
Profile 1	0.5980	0.0019	175.3
Profile 2	0.0536	0.0786	97.8
Profile 3	0.0051	0.0015	25.7

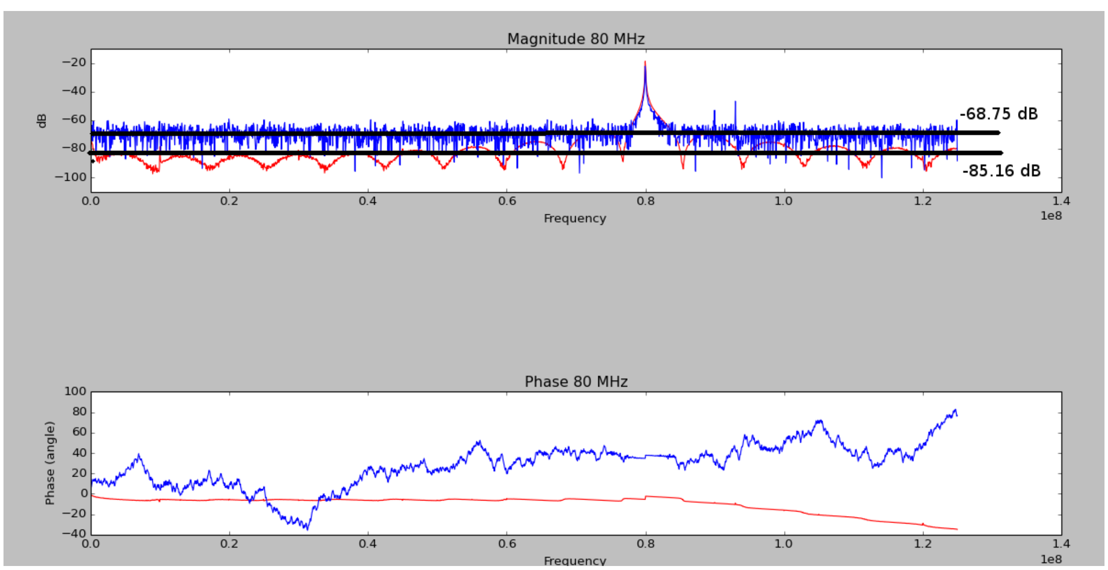
Table 2: Firmware Transfer Time

Profile Name	Time (s)	Throughput (Mbps)
Profile 0	.063	793.7
Profile 1	.101	990.1

4.3 Noise Performance

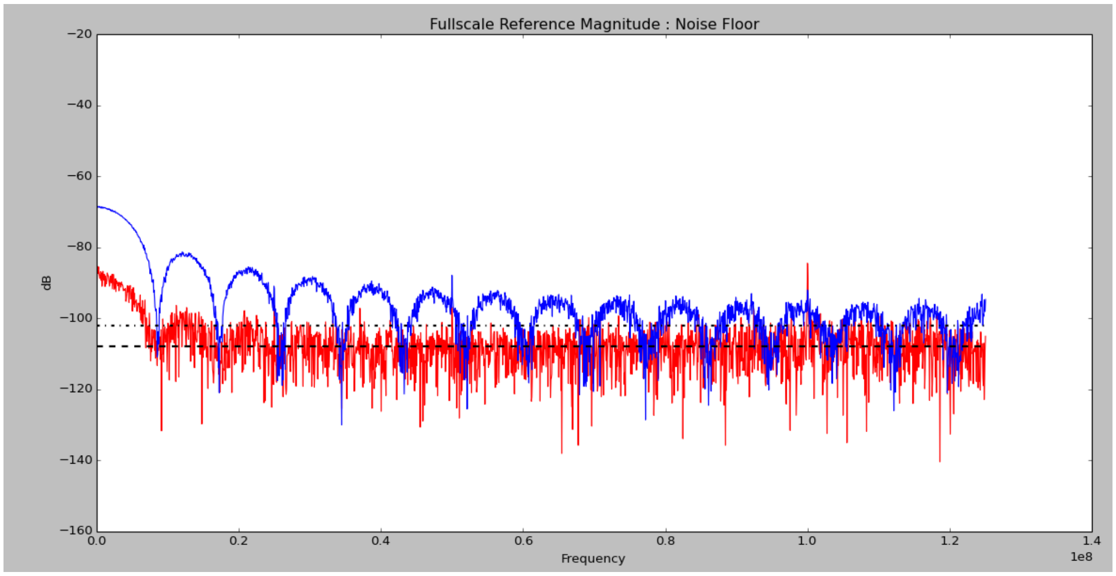
After analysing a few frequency domain signals we determined that in system, our noise floor for the reference channel is *-85.16 dB* and *-68.75 dB* for the channel which is fed from the APD and amplifier. This is illustrated in *Figure 4.* This however is not the proper noise figure for our ADC channels, but instead the noise floor of the entire system which they occur in. After the test we ran the system with nothing applied to the inputs of the ADC to attempt to quantify the noise floor of our ADC channels. This can be seen in *Figure 5* and resulted in a noise floor of -108 dB and -102 dB for the reference channel and measured channel respectively.

Figure 4: Noise Floor plotted on top of 80MHz



It is important to note that the scaling of the magnitude plot is the FFT of the signal normalized to the total dynamic range. In this case each point was divided by before it was converted to dB.

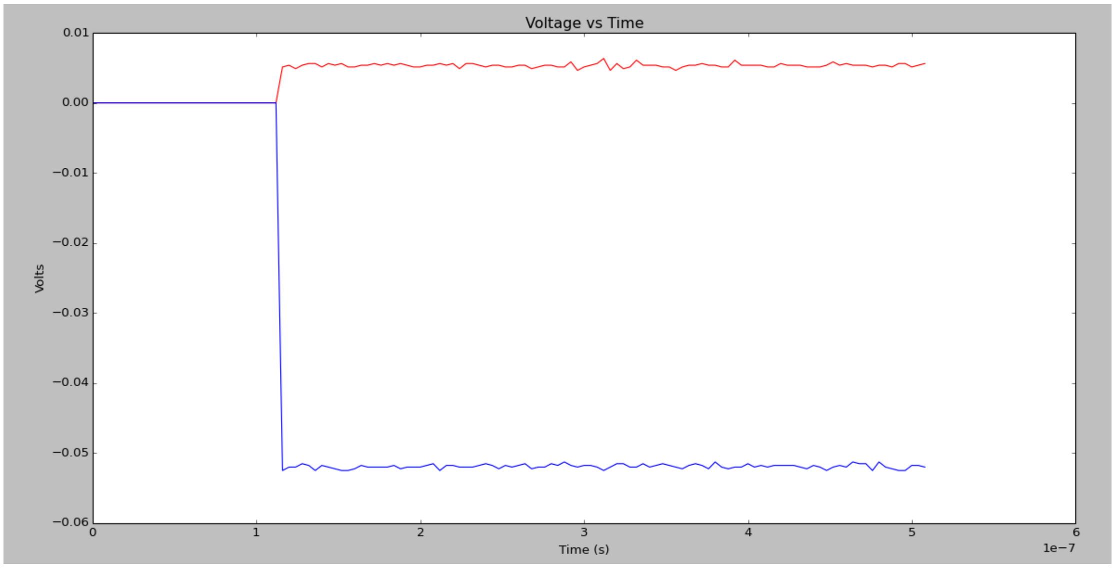
Figure 5: Noise Floor with no inputs to ADC



4.4 ADC and DDS Correctness

First we analyzed our DC performance with no inputs, this is displayed in *Figure 6* we found that the two channels have different offsets. The channels both have a DC offset, and are offset about apart with the reference channel at about and the reference channel at about . This offset could be due to mismatch in the termination resistors (one from each trace in the differential pair to a common bias point).

Figure 6: DC Performance with no inputs



In *Figure 7*, the time domain graph at a stimulus frequency of 60 MHz is plotted. This graph looks appropriate besides the lower frequency oscillations on the measured channel (blue). This oscillation is likely an artifact of the measurement setup.

Figure 7: Time Domain Graphs at 50 MHz

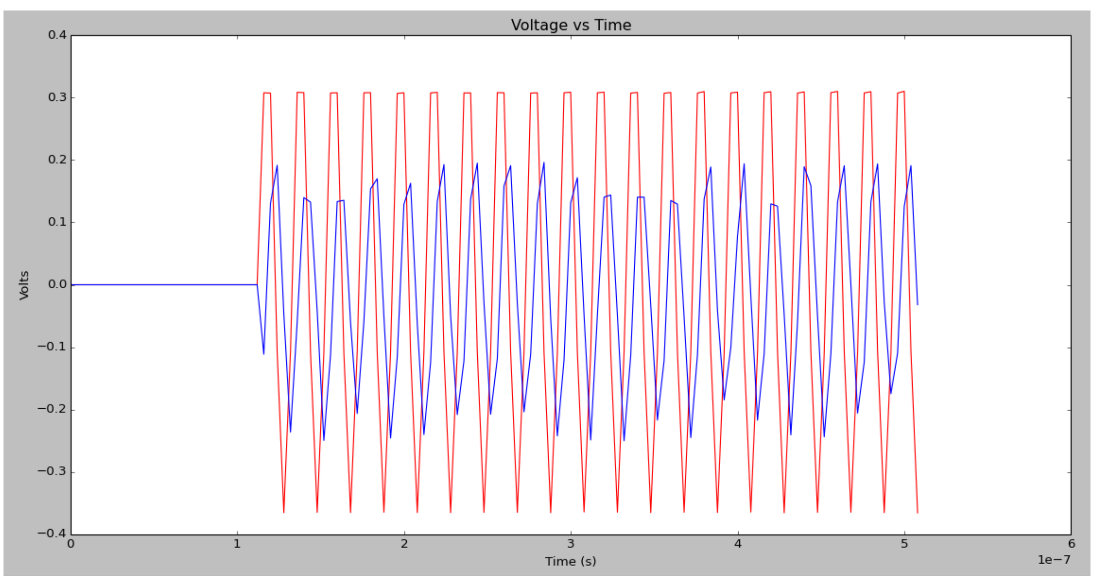


Figure 8 show the frequency domain plot. We notice some scalloping in the reference channel. This is interesting because in *Figure 6* the scalloping was in the other channel whose noise floor now sits above the scalloping that was present with no inputs applied. Currently we are not sure of the source of the scalloping in either case, however we are currently using a

rectangular windowing function which does have noticeable scalloping effects. This data was processed by taking the time domain information and taking an FFT with python and scipy. The results of the FFT were then normalized to the full scale magnitude value.

Figure 8: Frequency Domain Plots at 51 MHz

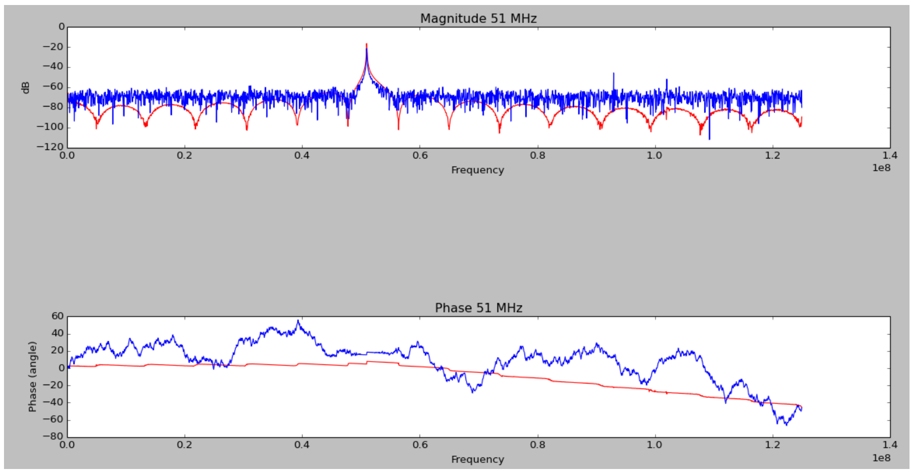
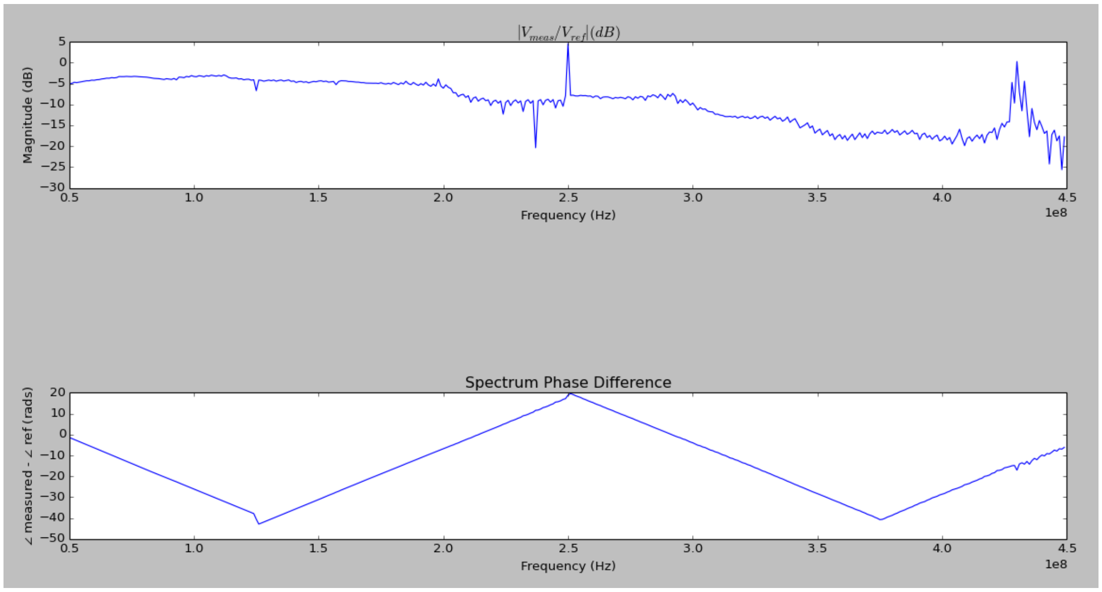


Figure 9, shows the transfer function essentially. We excited the system (using the DDS) in 1 MHz steps from 50 MHz to 450 MHz, we then recorded both a reference channel and the measurement channel after the optical system. We took the FFT and generated frequency domain plots like *Figure 8*. Since we knew where our frequency was we extracted the amplitude and phase information from the FFT and then plotted those in *Figure 9.* This is similar to the results of the Network Analyzer when that is used to provide the stimulus and report the S21 parameter.

Figure 9: "Transfer Function" of Measure at the different excitation frequencies



5 Conclusions

This test allowed us to demonstrate the the functionality of our first fully integrated system (hardware and software) and assess its performance. Our system successfully met many of the fundamental requirements that are listed in *Section 1.1* of our test plan. In *Section 4.1* of our test report, we listed various criteria for success. *Figure 3* shows that the hardware and software of our system successfully communicate and send meaningful data based on the controls (start frequency, step size, number of steps, etc) that were set by the user. Additionally, based on our calculations in *Section 4.2*, all of our data transfers were done in less than 1 second, this includes transferring 4kSamples/step at 400 steps in less than one second. *Figure 8* shows that our system produced a reasonable looking frequency response and that the peak is at the appropriate frequency (51 MHz). Therefore, based on these results, the system was successful and provided results comparable to prior systems.

6 Appendices

6.1 Appendix 1: Table of Technical Requirements as Specified in PDR Report

Requirement Name	**Parameters**
Frequency Range	50MHz-500MHz
Sample Size	14 Bits
Min Frequency Step Size	1MHz
Maximum Allowable Frequency Sweep Time for 4kSamples/step and 400steps	1s
Preferred Frequency Sweep Time	100ms at a sample size of 4kSamples/step and 450 steps
Max Sample Size	64kSamples/step
Max Steps	450 steps
Amplitude Error	±3% Amplitude Error
Phase Error	±0.1° Phase Error
Noise Floor	< -80dBm
ADC Input Impedance	50Ω
# of Simultaneous DDS Channels	6 Channels
Ethernet Speed	10/100/1000Mbps