Memo

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Team: Team #19: Team dDOSI

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Subject: Functional Test Plan

1 Test Overview

In this test we will be testing our integrated hardware and software, which includes two PCBs (the motherboard and the DDS frequency synthesis module), the microzed firmware and server and the Windows GUI and client code for interacting with the device. This test will take place in the customer's lab in ERB B05. We will perform a full optical test on an optical phantom with known characteristics. The data from this test will be used to analyze our systems accuracy compared to pre-existing systems. The test itself will involve setup (done before test begins), data collection and some basic data analysis to prove functionality and performance. Some of the more intensive data analysis for comparison will be done after the test is over.

1.1 Requirements

In *Appendix 1* (*Section 6.1*), the technical requirements as specified in our PDR report are listed with parameters for success. In this test we will be testing for the following system specifications:

- A frequency synthesis range from 50MHz to 450MHz
- ADC input bandwidth from 50MHz to 450MHz
- A average Sample Size of 4kSamples/step and a max size of 8kSamples/step.
- Minimum frequency step size of 1MHz
- The sweep time of under a second at 400 steps with 4kSamples/step (average case).
- An example user interface for our DLL.
- Noise floor less than -80dBm for the loop backed input.
- GUI functionality for setting samples, step size and other relevant configurations.
- Data storage to .csv file for processing in Excel, Matlab or other programs.
- Compatibility with current optical system.

1.2 Test Significance and Goals

This is the first full system test which includes both the hardware and software integrated into one usable package. This test has two major goals, one of them is to test the functionality and compatibility with the current system, the second is to test the performance of the device as used in system compared to previous measurement devices used by our customer. As described in *Section 1.1* this test will prove many of the fundamental requirements of our design and put us on the road to proving competitive performance with prior systems.

The test itself will include, using the software to talk to the hardware to configure and run a test, receiving the time domain information from the ADC, sending it to the software, and returning that time domain information into a comma-separated value (.csv) file. This process will show that the full workflow which we have specified works. Additionally, this process allows us to collect data and prove that our required data throughput is being met on both the communications and firmware ends. This test will prove the functionality of our hardware in system and is a major step towards meeting our goals of a successful full data transfer.

1.3 Criteria for Success

A successful test will include the following:

- Our hardware component successfully interfacing with the optical system we are measuring and stimulating.
- Our software successfully communicating with our hardware and returning meaningful data in the quantities, sizes, etc. which we specified.
- Firmware throughput at a rate matching the ethernet speed.
- A transfer of 4kSamples/step at 400 steps taking less than 1 second.
- A reasonable looking frequency domain response with a peak at the desired frequencies and minimal noise.

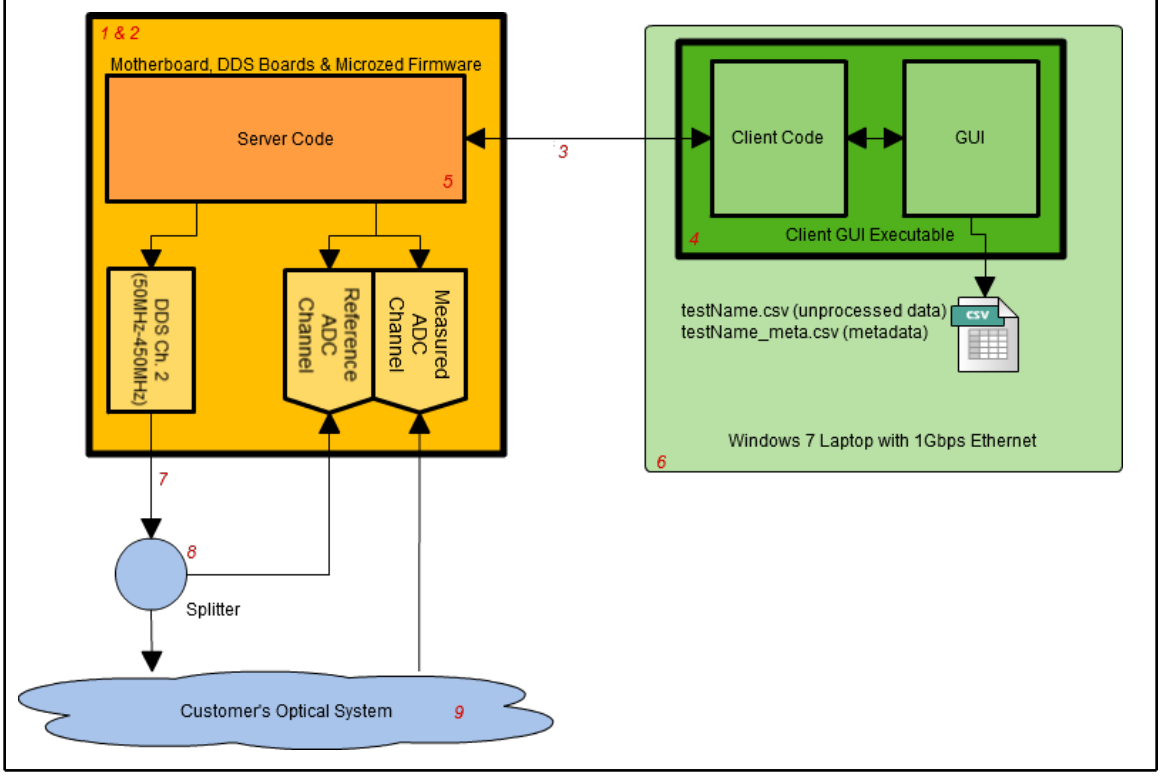
2 Equipment and Setup

2.1 Setup

The setup for our test is presented in *Figure 1*. The goal of this setup is to provide a functional test on a known working optical phantom. This way the data retrieved can be analysed by the researchers to be compared with previous systems.

In this system we see our two PCB's and the MicroZed, attached to a laptop running Windows 7 which is hosting our user facing client code. On the GUI, a profile containing information for the sweep (e.g. start frequency, step size, number of parameters, etc) is set up. This information is sent to the server code running on the MicroZed, which then starts a sweep. The output of our DDS will drive the input of a splitter which will split the signal to our reference ADC channel (CH. B) and the laser diode driver. After the sweep is done a *.csv* file with the unprocessed time domain data will be ready for analysis.

Figure 1: Diagram of Test



2.2 Equipment

As numbered in red in *Figure 1* we require the following equipment:

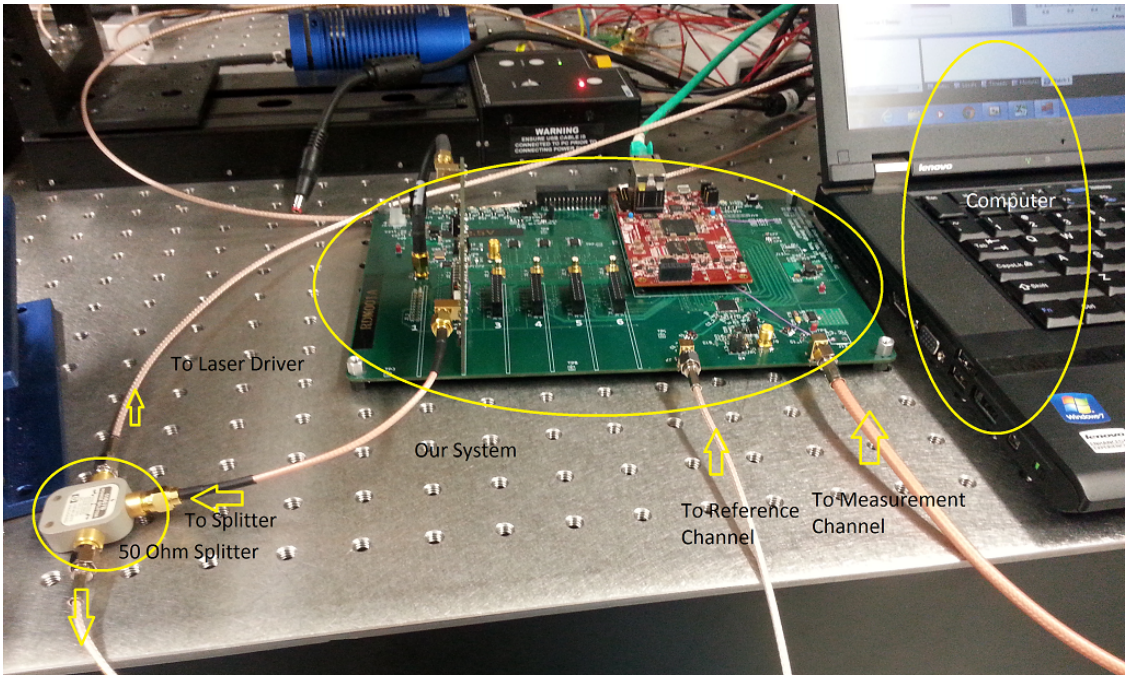
1. Motherboard PCB fully assembled, with MicroZed installed
2. DDS PCB fully assembled
3. Cat6 Ethernet Cable (1000Mbps)
4. Windows Executable for Client GUI
5. Server Code on SD Card for Microzed (includes FPGA .bit file)
6. Windows 7 Laptop with 1000Mbps Ethernet Link
7. 4 SMA cables for use with Darren's System
8. Splitter to generate reference and drive signal from DDS output
9. The optical system we are testing against

Additionally we will require 120VAC power to supply a 5V AC-DC switching power supply, and any other power requirements to run our customer's system. The system itself is composed of the following:

- An RF switch
- A laser diode driver

- An optical phantom with known characteristics
- An avalanche photodiode detector (with temperature compensation electronics)
- A broadband 40dB "gain block" amplifier (~10MHz-700MHz bandwidth)
- A computer for controlling the system

Figure 2: Picture of setup (with labels).



3 Measurement Plan

3.1 Measurement Procedures

Sections of testing:

1. Run without anything plugged into ADC to get a baseline for the noise floor. Run at different sample sizes. The profile is not very important for this test. The only element which truly matters is the Sample Size and preferably only 1 step is run.
2. Hook up ADC Channel B to the reference source, and Channel A to the return signal coming from the amplifier board. The setup is the one presented in *Figure 1* and *Figure 2*. This setup will be run under 4 different profiles
    a. Setup Profile 0, run 3 times
    b. Setup Profile 1, run 3 times
    c. Setup Profile 2, run 3 times
    d. Setup Profile 3, run 3 times

3.2 Profiles For Test

Table 1: Profiles with Relevant Settings

	Start Frequency (MHZ)	Step Size (MHz)	# of Steps	Sample Size (kS)
Profile 0	50	1	400	4
Profile 1	50	1	400	8
Profile 2	50	10	40	4
Profile 3	50	1	1	4

In *Table 1* the profiles for test are listed, each profile serves a purpose:

- Profile 0: Average case.
- Profile 1: Worst Case.
- Profile 2: A “fast” test, this may be used for obtaining multiple sweeps in a heartbeat, where granularity of the sweep is less important than the time domain information.
- Profile 3: Single transfer, used for overhead analysis.

We will run each profile 3 times to gather some statistics on the profile for analysis.

4 Data Collection

A majority of our data collection is automated because our Graphical User Interface (GUI) and related dynamic-link library (DLL) has the functionality to start an ADC sample and acquire it. It also has the ability to measure its own speed performance for analysis. The data collection itself will consist of setting up a run profile, which will be different for different tests, and clicking start. We will run multiple tests for each profile to gain some additional information for analysis and to acquire the appropriate statistics for analyzing our performance. The profiles being used are listed in *Section 3.2* with descriptions of why each one is being collected and analyzed.

The data will be collected into a binary file and then converted to a set of “.csv” files which can be used with almost any numeric analysis package, including, Python, Matlab, and Excel.

5 Assessment Procedure

There are two stages of assessment for this test. One functional and one performance based. The functional assessment will involve comparing the functionality of the current system against the full list of functions in the requirement list. The performance based assessment will involve comparing the data collection capabilities (accuracy and speed) of the new system against the old system as well as the requirements.

5.1 Ethernet and Software Performance and Functionality

After running the measurements the run time is recorded. This recorded run time is then logged into a spreadsheet for analysis. After a few runs we can histogram this file and determine how long it takes to run on average, and the standard deviation of the data. We expect a rather small standard deviation due to the point to point nature of our ethernet link. This data can be used to help guide parameters for a multi sweep system.

5.2 Firmware Throughput

To prove the viability of our hardware/firmware in potential future software systems (such as a linux to linux client server or the use of a different communications protocol) the firmware throughput will be measured. To meet the ethernet speed constraints a throughput of around 800 Mbit (matching standard 10/100/1000 ethernet throughputs) should be achieved on the firmware.

To measure this we will initiate a large sweep in the GUI (matching profile 1) and look at the packet timestamps with wireshark. Because each sweep is buffered on the MicroZed before it is sent to the client, the firmware throughput can be defined as the time between when the “start sweep” packet is received on the server and when the first data packet is sent by the server, divided by the total amount data collected.

5.3 Noise Performance

Due to the frequency domain nature of our analysis there are a few relevant noise parameters. One of them is the noise floor, which will be dependant on our sample size to some degree, and the other is the SNR (signal to noise ratio) which can be found from the noise floor. To analyze the noise floor we will take a set of measurements as per usual, normalize them and plot the frequency spectrum at a few steps. From this we will see a peak at a given frequency and then the noise floor below it. From this we can find the SNR and the noise floor.

A python script will analyze this data and return the number during the test for analysis, you could also histogram the values over multiple sweeps to get a better feel for what the noise actually looks like.

5.4 ADC and DDS Correctness

We need to use the data collected to prove that the DDS is being set correctly and the ADC is working correctly. One way to do this is through a loopback test, where the DDS is hooked directly to an ADC channel and measured from there. This is reasonable, but testing in system can provide similar results about the correctness of the system because we always have a reference channel. To prove correctness we will take the data from a sweep and plot it at key steps in the sweep. We will also plot the frequency domain information to view the frequency which is strongest and verify that that peak is where we believe it should be. Another way to do this would be to do the analysis completely in the time domain, however, our end results really only care about the frequency domain information, and once we are subsampling, the time domain information becomes less useful.

5.5 Comparison to Previous Systems

We will compare the functionality and performance of our system with our customer's previous systems. In order to do this we must take our data and extract the phase and amplitude data at each frequency step. In order to effectively analyze this we must first calibrate against a known sample. We can then figure out the response of the overall system, including the cables, amplifiers and APD. Once we have a calibration and the amplitude and phase information we can apply our data to that which our customer currently gets from his network analyzer.

We are responsible for the data collection and formatting it so that it can be used in our customer's MATLAB scripts. Comparison may take longer than the time between the test plan and test report but will be done for the final report.

6 Appendices

6.1 Appendix 1: Table of Technical Requirements as Specified in PDR Report

Requirement Name	Parameters
Frequency Range	50MHz-500MHz
Sample Size	14 Bits
Min Frequency Step Size	1MHz
Maximum Allowable Frequency Sweep Time for 4kSamples/step and 400steps	1s
Preferred Frequency Sweep Time	100ms at a sample size of 4kSamples/step and 450 steps
Max Sample Size	64kSamples/step
Max Steps	450 steps
Amplitude Error	±3% Amplitude Error
Phase Error	±0.1° Phase Error
Noise Floor	< -80dBm
ADC Input Impedance	50Ω
# of Simultaneous DDS Channels	6 Channels
Ethernet Speed	10/100/1000Mbps