HCAL DCC Buffering

128k x 32 FIFOs

SDRAM buffer
128 events x 18 HTRs
(512x32 each)

PCI-1

Tag FIFOs

Event Builder

PCI-2

S-Link FIFO

Monitor buffer
128 events

S-Link currently runs at 32MHz
(256 mbyte/sec)

18 FIFOs
Header info for each event

L1A FIFO ~ 1k evt

L1A FIFO flags used to generate TTS overflow warning (programmable upper/lower limits)

E. Hazen – RUWG Mar 2004
Are 5 thresholds in buffer levels needed to control this state machine?