DCC Simplification

• Proposal in a nutshell:
  – Simplify DCC before completing production
  – One PCB: No more LRBs, logic boards, etc
  – Cost neutral or savings

• Why do this now?
  – Not enough motherboards or LRBs available for spares and test stands
    • Production now expensive / difficult (obsolete parts)
  – Firmware maintenance is a problem
    • 3 designers, 6 distinct designs, mixed vendors
    • PCI busses are complicated and not as useful as originally foreseen
  – Long-term reliability is in doubt
Block Diagram

4 HTR inputs

Spartan 3 FPGA

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Event Builder FPGA

XC4VLX25-4FF668

DDR2 SDRAM

VME64xP (Buffers)

SLink64

Maryland TTCrx Mezzanine

CPLD

Flash

US CMS - Fermilab - Nov 2004 E. Hazen
Some Technical Details

- Spartan-3 can de-serialize channel-link signals
  - Tested by us in Virtex 2 so far
    (technique described in Xilinx app notes)

- Burst data rate of $40\text{MHz} \times 2 \times 12 = 960\text{MB/sec}$ can easily be handled by DDR memory

- Virtex 4 simplifies DDR interface (V-2 ok too)
  - Available now: already have 10pc in stock

- Software is much simpler without PCI busses
  - Can comply with C. Schwick's rules - VME64xP

- All significant logic on one FPGA

- Event builder firmware largely unchanged
  - Significant simplification by removing PCI busses
Fewer Parts

Current DCC has a big stack of daughter-boards. This made sense when we started. In the long run this is likely to be a reliability problem.

New design would have many fewer parts and only two daughterboards.

- Single-width module (gain 2 slots per crate)
- Much simpler mechanics
Summary

- Proposed mods make production and maintenance much simpler
- Impact on M&S cost is negligible - new DCCs are much cheaper
- Little new firmware is needed
- Can comply with CMS VME rules - simpler software
- Prototype could be ready before end of 2004